LECTURE NOTES

ON

LINEAR INTEGRATED CIRCUITS

2022 – 2023
T. E. V Semester

ELECTRONICS
(Mumbai University-R19)

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DESIGN WITH LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

Course Objectives:

- *Design of OPAMPS, Classification of OPAMPs.*
- *To study and design various Linear applications of OPAMPs.*
- *To study and design various Non- linear applications of OPAMPs*

Course Outcomes:

- *Understand the basic building blocks of linear integrated circuits and its characteristics.*
- *Analyze the linear, non-linear and specialized applications of operational amplifiers.*
- *Understand the theory of ADC and DAC.*
- *Realize the importance of Operational Amplifier.*

UNIT – I

Differential Amplifiers: Differential amplifier configurations, Balanced and unbalanced output differential amplifiers, current mirror, level Translator.

Operational amplifiers: Introduction, Block diagram, Ideal op-amp, Equivalent Circuit, Voltage Transfer curve, Open loop op-amp configurations. Introduction to dual OP-AMP TL082 as a general purpose JFET-input Operational Amplifier.

UNIT-II

Introduction, feedback configurations, voltage series feedback, voltage shunt feedback and differential amplifiers, properties of Practical op-amp.

Frequency response: Introduction, compensating networks, frequency response of internally compensated op-amps and non-compensated op-amps, High frequency op-amp equivalent circuit, open loop gain Vs frequency, closed loop frequency response, circuit stability, slew rate.

UNIT-III

DC and AC amplifiers, peaking amplifier, summing, scaling and averaging amplifiers, instrumentation amplifier, voltage to current converter, current to voltage converter, integrator, differentiator, active filters, First, Second and Third order Butterworth filter and its frequency response, Tow-Thomas biquad filter.

UNIT-IV

Oscillators, Phase shift and wein bridge oscillators, Square, triangular and sawtooth wave generators, Comparators, zero crossing detector, Schmitt trigger, characteristics and limitations.

Specialized applications: 555 timer IC (monostable & astable operation) & its applications, PLL, operating principles, Monolithic PLL, applications, analog multiplier and phase detection, Wide bandwidth precision analog multiplier MPY634 and its applications.

UNIT V

Analog and Digital Data Conversions, D/A converter – specifications – weighted
resistor type, R-2R Ladder type, Voltage Mode and Current-Mode -2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications – Flash type – Successive Approximation type – Single Slope type – Dual Slope type – A/D Converter using Voltage-to-Time Conversion –Over-sampling A/D Converters,

TEXT BOOKS:

D. Roy Chowdhury, "Linear Integrated Circuits", New Age International (p) Ltd, 2nd Edition, 2003.

K .LalKishore, "Operational Amplifiers and Linear Integrated Circuits", Pearson Education,200 7.

REFERENCES:

Ramakanth A. Gayakwad, "Op-Amps & Linear ICs", PHI, 4th edition, 1987.

R.F.Coughlin & Fredrick Driscoll, "Operational Amplifiers & Linear Integrated Circuits", 6th Edition, PHI.

David A. Bell, "Operational Amplifiers & Linear ICs", Oxford University Press, 2nd edition, 2010.

UNIT-I

1.1 OPERATIONAL AMPLIFIER (OP-AMP):

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package.

The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, and others.

1.2 Ideal op-amp:

An ideal op-amp would exhibit the following electrical characteristics:

1. **Infinite voltage gain.**
2. **Infinite input resistance so that almost any signal source can drive it and there is no loading on the preceding stage.**
3. **Zero output resistance Ro so that output can drive an infinite number of other devices.**
4. **Zero output voltage when input voltage is zero.**
5. **Infinite bandwidth so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.**
6. **Infinite common mode rejection ratio so that the output common-mode noise voltage is zero.**
7. **Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.**

1.3 Equivalent circuit of an op-amp:

Fig. 1.1 shows an equivalent circuit of an op-amp. V1 and V2 are the two input voltage voltages. Ri is the input impedance of OPAMP. Ad Vd is an equivalent Thevenin's voltage source and Ro is the Thevenin's equivalent impedance looking back into the terminal.

This equivalent circuit is useful in analysing the basic operating principles of op-Amp and in observing the effects of standard feedback arrangements.

$$VO = Ad (V1-V2) = AdVd.$$

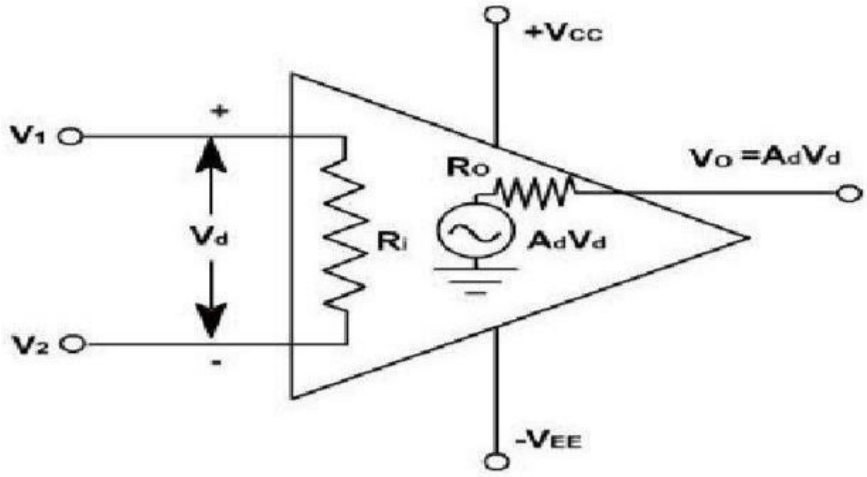

Fig 1.1: Equivalent circuit of OP-AMP

This equation indicates that the output voltage Vo is directly proportional to the algebraic difference between the two input voltages. In other words the opamp amplifies the difference between the two input voltages. It does not amplify the input voltages themselves. The polarity of the output voltage depends on the polarity of the difference voltage Vd.

1.4 Ideal Voltage Transfer Curve:

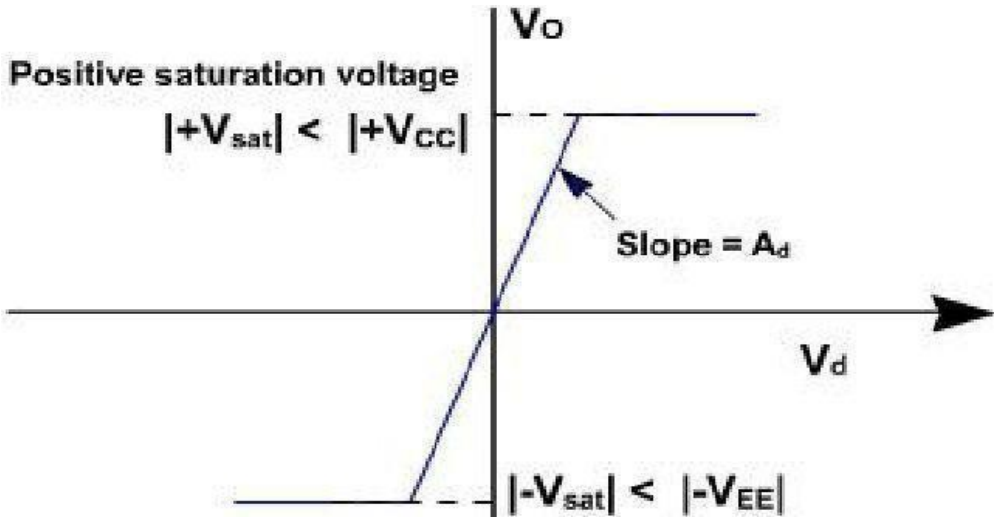

Fig 1.2: Ideal voltage transfer curve

The graphic representation of the output equation is shown in fig.1.2 in which the output voltage Vo is plotted against differential input voltage Vd, keeping gain Ad constant. The output voltage cannot exceed the positive and negative saturation voltages. These saturation voltages are specified for given values of supply voltages. This means that the output voltage is directly proportional to the input difference voltage only until it reaches the saturation voltages and thereafter the output voltage remains constant. Thus curve is called an ideal voltage transfer curve, ideal because output offset voltage is assumed to be zero. If the curve is drawn to scale, the curve would be almost vertical because of very large values of Ad.

1.5 INTERNAL CIRCUIT :

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MHz to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

The internal block diagram of an op-amp is shown in the fig 1.3. The input stage is the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. On most amplifiers, the intermediate stage is dual input, unbalanced output. Because of direct coupling, the dc voltage at the output of the intermediate stage is well above ground potential. Therefore, the level translator (shifting) circuit is used after the intermediate stage downwards to zero volts with respect to ground. The final stage is usually a push pull complementary symmetry amplifier output stage. The output stage increases the voltage swing and raises the ground supplying capabilities of the op-amp. A well designed output stage also provides low output resistance.

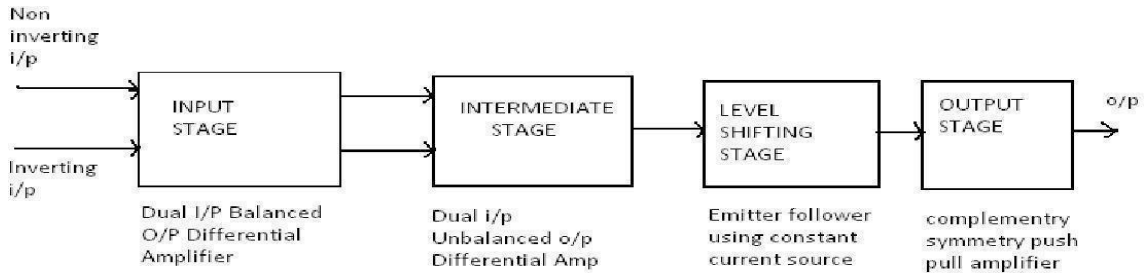

Fig 1.3: Block Diagram of OP-AMP

1.6 Differential amplifier:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals. The two transistors Q1 and Q2 have identical characteristics. The resistances of the circuits are equal, i.e. RE1 = R E2, RC1 = R C2 and the magnitude of +VCC is equal to the magnitude of -VEE. These voltages are measured with respect to ground.

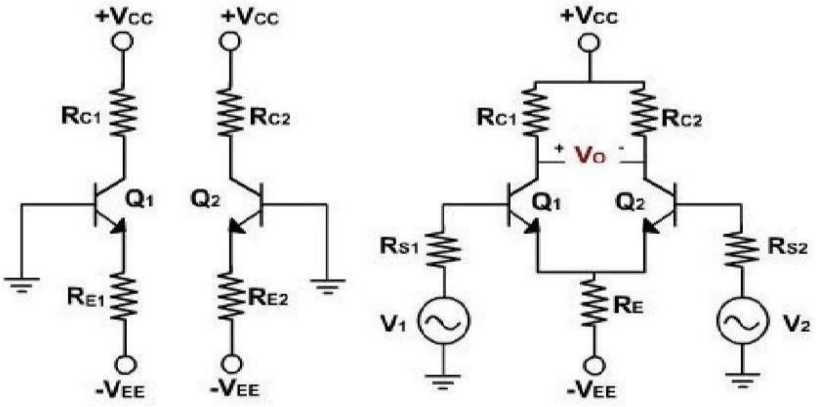

Fig 1.4: Differential Amplifier

To make a differential amplifier, the two circuits are connected as shown in fig. 1.4. The two +VCC and -VEE supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of RE1 and RE2 is replaced by a resistance RE. The two input signals v1& v2 are applied at the base of Q1 and at the base of Q2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by RC = RC1 = RC2.

Ideally, the output voltage is zero when the two inputs are equal. When v1 is greater then v2 the output voltage with the polarity shown appears. When v1 is less than v2, the output voltage has the opposite polarity.

The differential amplifiers are of different configurations.

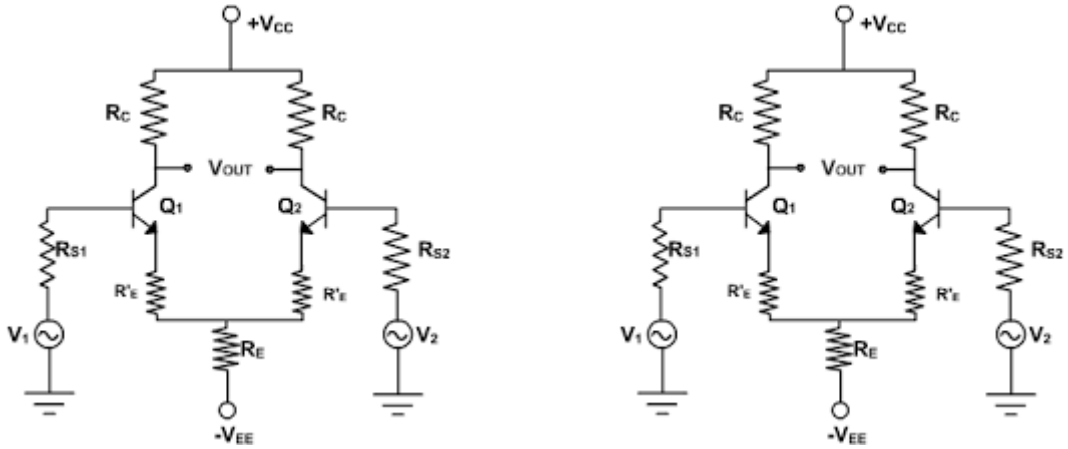

Fig 1.5: Dual input, balanced output differential amplifier.

Fig.1.6.Dual input, unbalanced output differential amplifier

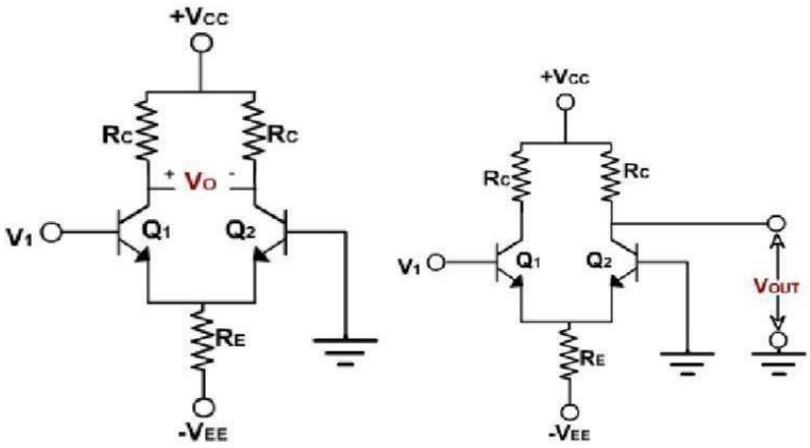

Fig 1.6:Single input, balanced output differential amplifier

Fig.1.8.Single input, unbalanced output differential amplifier.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.

2. Dual input, unbalanced output differential amplifier.

3. Single input balanced output differential amplifier.

4. Single input unbalanced output differential amplifier.

These configurations are shown in fig(1.5,1.6,1.7, 1.8), and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output. A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signal

1) Dual Input, Balanced Output Differential Amplifier:

The circuit is shown in fig.1.10V1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

1.6.1 D.C. Analysis:

To obtain the operating point (ICQ and VCEQ) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages V1 and V2 to zero as shown in fig1.9.

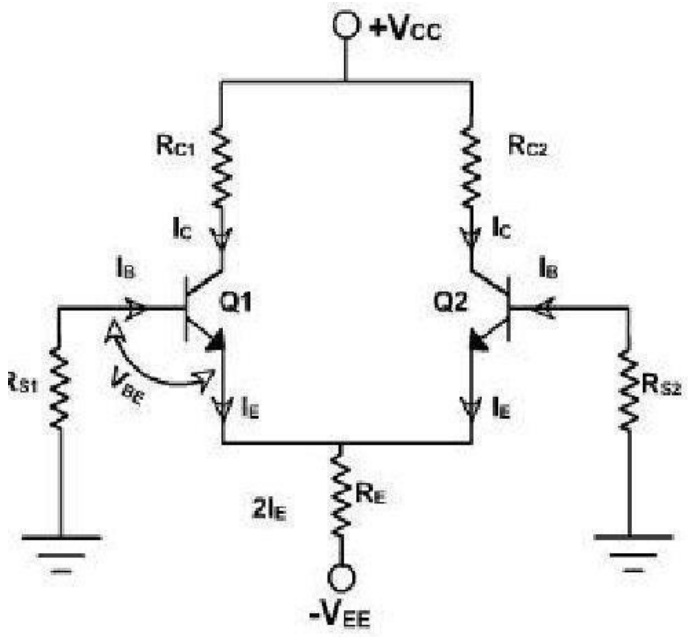

Fig 1.7: Differential Amplifier

The internal resistances of the input signals are denoted by RS because RS1= RS2. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of ICQ and VCEQ can be used for second transistor Q2. Applying KVL to the base emitter loop of the transistor Q1.

$$R_S I_B + V_{BE} + 2 I_E R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (=1)$$

$V_{BE} = 0.3V$ for Si and $0.2V$ for Ge.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{DC}}{2R_E}$$

The value of RE sets up the emitter current in transistors Q1 and Q2 for a given value of VEE. The emitter current in Q1 and Q2 are independent of collector resistance RC. The voltage at the emitter of Q1 is approximately equal to -VBE if the voltage drop across R is negligible. Knowing the value of IC the voltage at the collector VC is given by

VC =VCC- IC RC and VCE = VC- VE

=VCC - IC RC + VBE VCE = VCC + VBE - ICRC

From the two equations VCEQ and ICQ can be determined.

This dc analysis is applicable for all types of differential amplifier

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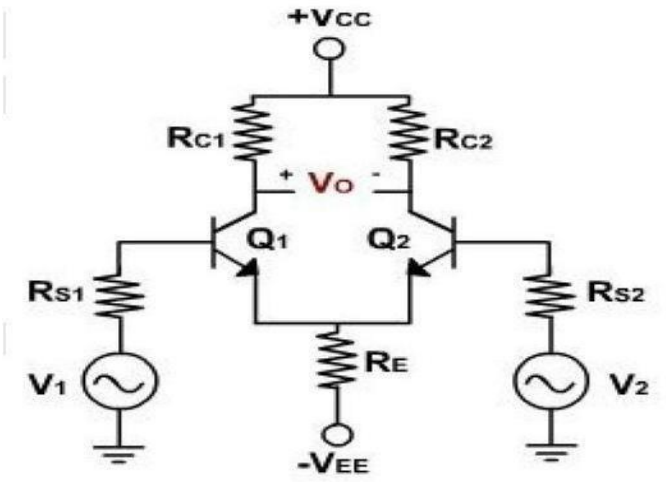


1.6.2 A.C. Analysis :

The circuit is shown in fig.1.10 V1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

Dc analysis has been done to obtain the operating point of the two transistors. To find the voltage gain Ad and the input resistance Ri of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown infig1.11. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

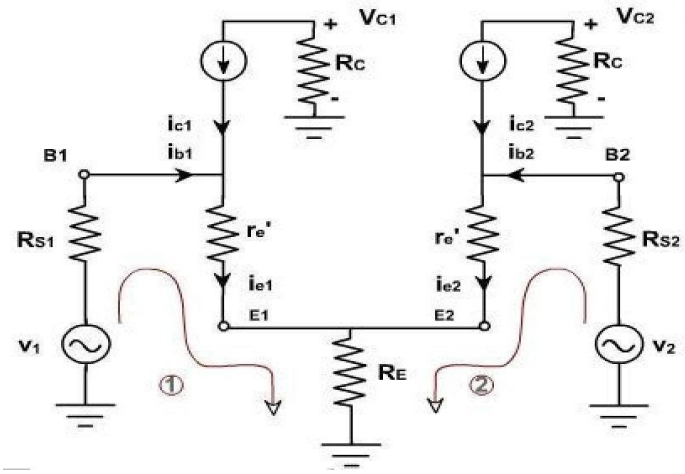


Fig 1.9: Differential Amplifier A/C Analysis

Since the two dc emitter currents are equal. Therefore, resistance r'e1 and r'e2 are also equal and designated by r'e . This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages v1 and v2. This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector C2 is assumed to be more positive with respect to collector C1 even though both are negative with respect to ground.

The output voltage VO is given by

$$\begin{aligned} V_o &= V_{c2} - V_{c1} \\ &= -R_C i_{C2} - (-R_c i_{c1} \\ &= R_C(i_{C1} - i_{c2}) \\ &= R_C(i_{e1} - i_{e2}) \end{aligned}$$

Substituting ie1, & ie2 in the above expression

$$V_o = R_C\left\{\frac{(r_e' + R_E)V_1 - R_E V_2}{(r_e' + R_E)^2 - R_E^2} - \frac{(r_e' + R_E)V_2 - R_E V_1}{(r_e' + R_E)^2 - R_E^2}\right\}$$

$$= \frac{R_C(V_1 - V_2)(r_e' - 2R_E)}{r_e'(r_e' + 2R_E)}$$

$$V_o = \frac{R_C}{r_e'}(V_1 - V_2) \ldots\ldots\ldots\ldots E(1)$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as Vd =V1-V2 the voltage gain of the dual input balanced output differential amplifier can be given by (E-2).

1.6.3 Differential Input Resistance:

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance Ri1 seen from the input signal source V1 is determined with the signal source V2 set at zero.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

$$R_{i1} = \frac{\beta r'_e(r'_e + 2R_E)}{r'_e + R_E}$$

Since $R_E >> r'_e$

$\therefore \quad r'_e + 2R_E >> 2R_E$

Similarly, the input signal V1 set at zero to determine the input resistance Ri2 seen from the input signal source V2. Resistance RS1 and RS2 are ignored because they are very small. Substituting ie1,

Similarly

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{v_1=0}$$

$$= \left.\frac{V_2}{i_{e2} / \beta}\right|_{v_1=0}$$

$$R_{i2} = 2\beta r'_e \qquad (E-4)$$

The factor of 2 arises because the re' of each transistor is in series. To get very high input impedance with differential amplifier is to use Darlington transistors. Another ways is to use FET.

1.6.4 Output Resistance:

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance RO1 measured between collector C1 and ground is equal to that of the collector resistance RC. Similarly the output resistance RO2 measured at C2 with respect to ground is equal to that of the collector resistor RC.

RO1 = RO2 = RC (E-5)

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

2) Dual Input, Unbalanced Output Differential Amplifier:

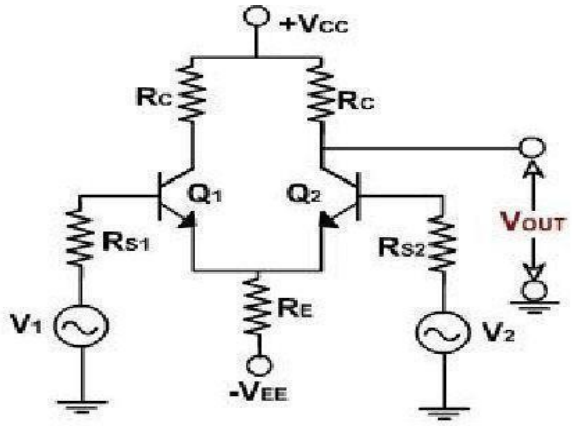


Fig 1.10: Differential Amplifier

In this case, two input signals are given however the output is measured at only one of the two- collector w.r.t. ground as shown in fig1.12. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground.

In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_2/\beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ}R_C$$

AC Analysis:

The output voltage gain in this case is given by

$$A_d = \frac{V_0}{V_d} = \frac{R_C}{2r_e}$$

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since at the output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

1.7 Level Translator:

Because of the direct coupling the dc level at the emitter rises from stages to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

To shift the output dc level to zero, level translator circuits are used. An emitter follower with voltage divider is the simplest form of level translator as shown in fig 1.13. Thus a dc voltage at the base of Q produces 0V dc at the output. It is decided by R1 and R2. Instead of voltage divider emitter follower either with diode current bias or current mirror bias as shown in fig 1.14may be used to get better results.

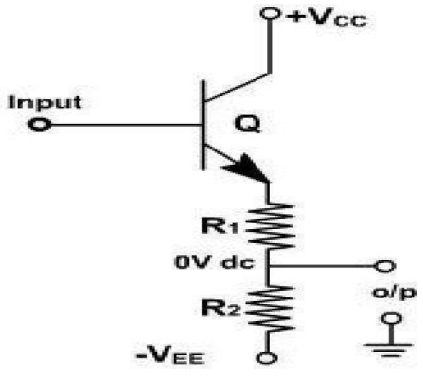


Fig 1.11: Common collector Amplifier

In this case, level shifter, which is common collector amplifier, shifts the level by 0.7V. If this shift is not sufficient, the output may be taken at the junction of two resistors in the emitter leg.

Fig.1.15 shows a complete op-amp circuit having input different amplifiers with balanced output, intermediate stage with unbalanced output, level shifter and an output amplifier.

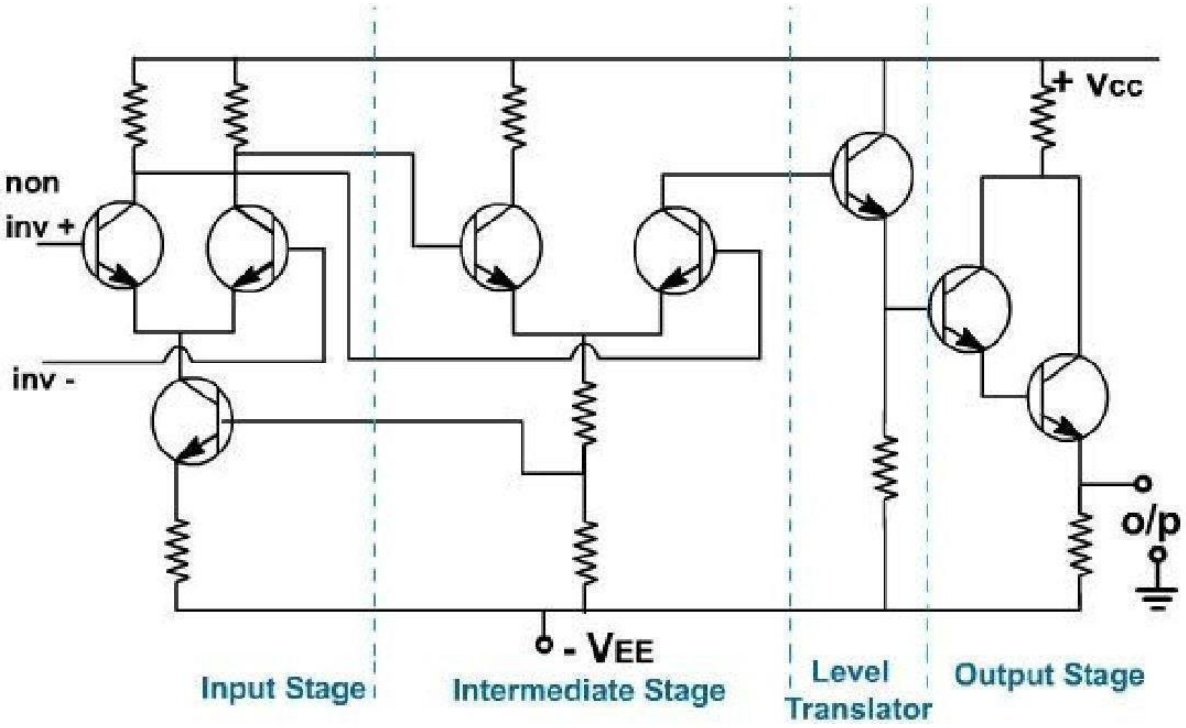


Fig 1.12: Circuit Diagram of OP-AMP

UNIT II

1.8 OP-AMP CHARACTERISTICS

1.8.1 DC CHARACTERISTICS:

a) Input offset voltage:

Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. Let us denote the output offset voltage due to input offset voltage Vio as Voo. The output offset voltage Voo is caused by mismatching between two input terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characteristics. This means that the collector currents in these two transistors are not equal which causes a differential output voltage from the first stage. The output of first stage is amplified by following stages and possibly aggravated by more mismatching in them.

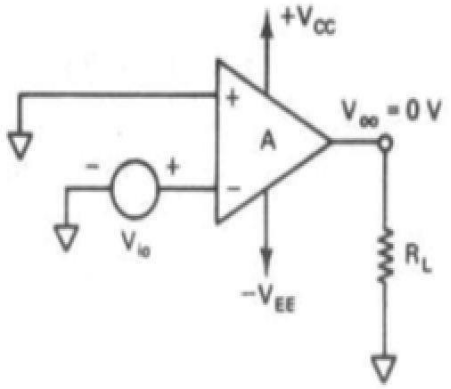


Fig 1.13: Input offset voltage in op-amp

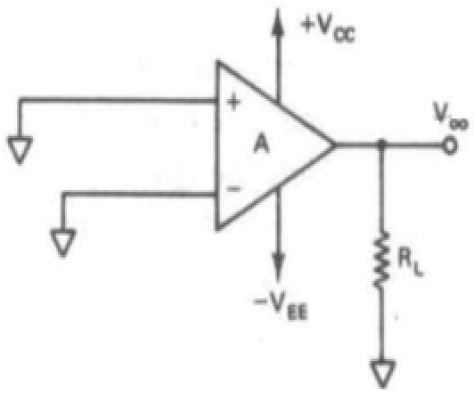


Fig 1.17 Output offset voltage in op-amp

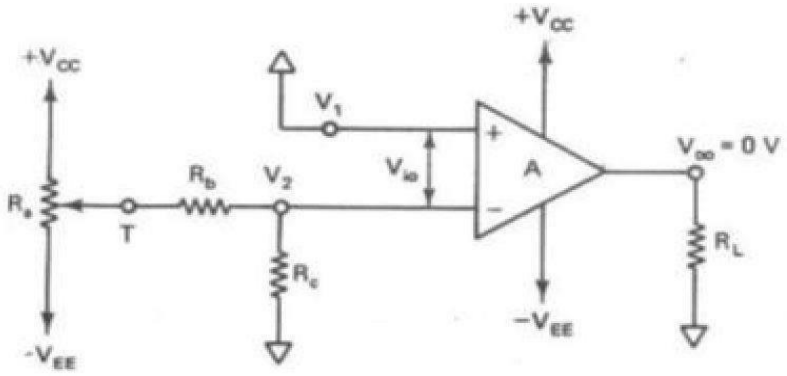


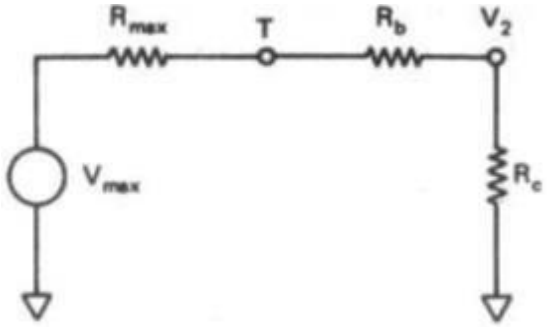
Fig 1.14:.Op-Amp with offset voltage compensating network

The op-amp with offset-voltage compensating network is shown in Figure1.18. The Compensating network consists of potentiometer *Ra* and resistors *Rb* and *Re.* To establish a relationship between *Vio,* supply voltages, and the compensating components, first Thevenize the circuit, looking back into *Ra* from point *T.* The maximum Thevenin's equivalent resistance *Rmax,* occurs when the wiper is at the center of the Potentiometer, as shown in Figure.

Rmax =(R a /2)||(R a /2)

Supply voltages *VCC* and *–VEE* are equal *in* magnitude therefore; let us denote their magnitude by voltage *V.*

Thus Vmax= *V.*



where *V2* has been expressed as a function of maximum Thevenin's voltage *Vmax* and maximum Thevenin's resistance, But the maximum value of *V2* can be equal to *Vio* since *V1*

— *V2* = *Vio.* Thus Equation becomes

$$V_2 = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

$$V_{io} = \frac{R_c}{R_{max} + R_b + R_c} V_{max}$$

Assume Rb >Rmax >Rc, where Rmax = Ra/4.
Using this assumption Rmax+Rb+Rc=Rb

There

$$V_{io} = \frac{R_c V_{max}}{R_b}$$

where

$$V_{max} = V = |V_{CC}| = |-V_{EE}|$$

$$V_{io} = \frac{R_c V}{R_b}$$

Let us now examine the effect of *Vio* in amplifiers with feedback. The non-inverting and inverting amplifiers with feedback are shown in Figure.1.19. To determine the effect of Vio, in each case, we have to reduce the input voltage vin to zero.

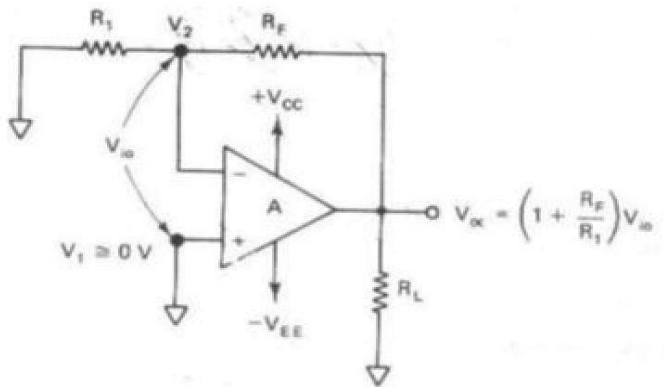


Fig 1.15: Closed loop non inverting or inverting Amp

With vin reduced to zero, the circuits of both non-inverting and inverting amplifiers are the sameas the circuit in Figure. The internal resistance Rin of the input signal voltage is negligibly small. In the figure, the non-inverting input terminal is connected to ground; therefore, assume voltage*V1* at input terminal to be zero. The voltageV2 at the inverting input terminal can be determinedby applying the voltage-divider rule:

$$V_2 = \frac{R_1 V_{oo}}{R_1 + R_F}$$

Therefore,

$$V_{oo} = \frac{R_1 + R_F}{R_1} V_2$$

Since $V_{io} = |V_1 - V_2|$ and $V_1 = 0$ V,

$$V_{io} = |0 - V_2| = V_2$$

Therefore,

$$V_{oo} = \left(1 + \frac{R_F}{R_1}\right) V_{io} = (A_{oo})\, V_{io}$$

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

b) Input bias current : Input bias current IB as the average value of the base currents entering into terminal of an op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

where I_{B1} = dc bias current flowing into the noninverting input
I_{B2} = dc bias current flowing into the inverting input

IB=IB1=IB2

Obtaining the expression for the output offset voltage caused by the input bias current IB in the inverting and non-inverting amplifiers and then devise some scheme to eliminate or minimize it.

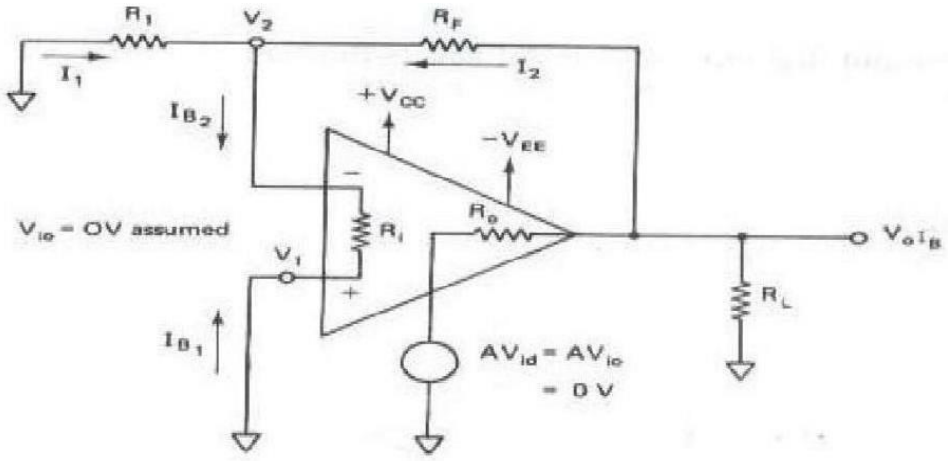


Fig 1.16: practical Op-Amp

In the figure, the input bias currents ‘81 and *1* are flowing into the non-inverting and inverting input leads, respectively. The non-inverting terminal is connected to ground; therefore, the voltage *V1* = 0 V. The controlled voltage source *A Vio* =0 V since Vio= 0 V is assumed. With output resistance Ro is negligibly small, the right end of *RF* is essentially at ground potential; that is, resistors *R1*, and *RF* are in parallel and the bias current *I,* flows through them. Therefore, the voltage at the inverting terminal is d) Thermal Drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25oc may not remain so when the temperature rises to 35oc. This is called thermal drift.

1.8.2 AC CHARACTERISTICS:

a) Slew Rate

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-**amp's output voltage** should change instantaneously in response to input step voltage. The symbolic diagram of an OPAMP is shown in fig 1.21

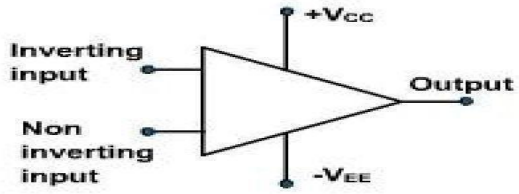


Fig 1.17: Op-Amp Symbol

Need for frequency compensation in practical op-amps:

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods: a) Dominant- pole compensation b) Pole- zero compensation.

741c is most commonly used OPAMP available in IC package. It is an 8-pin DIP chip.

Performance Parameters/ Characteristics of OP-AMP :

1. **Input Offset Voltage:**

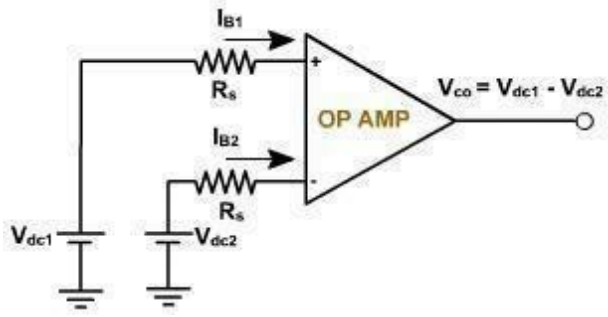


Fig 1.18: Input offset voltage

If no external input signal is applied to the op-amp at the inverting and non-inverting terminals the output must be zero. That is, if Vi=0, Vo=0. But as a result of the given biasing supply voltages, +Vcc and –Vcc, a finite bias current is drawn by the op-amps, and as a result of asymmetry on the differential amplifier configuration, the

output will not be zero. This is known as offset. Since Vo must be zero when Vi=0 an input voltage must be applied such that the output offset is cancelled and Vo is made zero. This is known as input offset voltage. Input offset voltage (Vio) is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output voltage. Fig 1.22 shows that two dc voltages are applied to input terminals to make the output zero.

$$Vio = Vdc1 - Vdc2$$

Vdc1 and Vdc2 are dc voltages and RS represents the source resistance. Vio is the difference of Vdc1 and Vdc2. It may be positive or negative. For a 741C OPAMP the maximum value of Vio is 6mV. It means a voltage ± 6 mV is required to one of the input to reduce the output offset voltage to zero. The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched.

2. Input offset Current:

Though for an ideal op-amp the input impedance is infinite, it is not so practically. So the IC draws current from the source, however smaller it may be. This is called input offset current Iio. The input offset current Iio is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier as shown in fig 1.22.

$$Iio = | IB1 - IB2 |$$

The Iio for the 741C is 200nA maximum. As the matching between two input terminals is improved, the difference between IB1 and IB2 becomes smaller, i.e. the Iio value decreases further. For a precision OPAMP 741C, Iio is 6 nA

3. Input Bias Current:

The input bias current IB is the average of the current entering the input terminals of a balanced amplifier i.e.

$$IB = (IB1 + IB2) / 2$$

For ideal op-amp IB=0. For 741C IB(max) = 700 nA and for precision 741C IB = ± 7 nA

4. Differential Input Resistance: (Ri)

Ri is the equivalent resistance that can be measured at either the inverting or non-inverting input terminal with the other terminal grounded. For the 741C the input resistance is relatively high 2 MΩ. For some OPAMP it may be up to 1000 G ohm**.**

5. Input Capacitance: (Ci)

Ci is the equivalent capacitance that can be measured at either the inverting and non inverting terminal with the other terminal connected to ground. A typical value of Ci is 1.4 pf for the 741C.

6. Offset Voltage Adjustment Range:

741 OPAMP have offset voltage null capability. Pins 1 and 5 are marked offset null for this purpose. It can be done by connecting 10 K ohm pot between 1 and 5.

By varying the potentiometer, output offset voltage (with inputs grounded) can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying 10 K pot. For the 741C the offset voltage adjustment range is ± 15 mV.

7. Input Voltage Range :

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and non-inverting input terminals. For the 741C, the range of the input commo
mode voltage is ± 13V maximum. This means that the common mode voltage applied at both input terminals can be as high as +13V or as low as -13V.

8. Common Mode Rejection Ratio (CMRR).

CMRR is defined as the ratio of the differential voltage gain Ad to the common mode voltage gain

ACM CMRR = Ad / ACM.

For the 741C, CMRR is 90 dB typically. The higher the value of CMRR the better is the matching between two input terminals and the smaller is the output common mode voltage.

9. Supply voltage Rejection Ratio: (SVRR)

SVRR is the ratio of the change in the input offset voltage to the corresponding change in power supply voltages. This is expressed inΔV / V or in decibels, SVRR can be defined as

$$SVRR = \Delta Vio / \Delta V$$

Where ΔV is the change in the input supply voltage and ΔVio is the corresponding change in the offset voltage. For the 741C, SVRR = 150 μ V / V.

For 741C, SVRR is measured for both supply magnitudes increasing or decreasing simultaneously, with R3= 10K. For same OPAMPS, SVRR is separately specified as positive SVRR and negative SVRR.

10. Large Signal Voltage Gain:

Since the OPAMP amplifies difference voltage between two input terminals, the voltage gain of the amplifier is defined as

$$\text{Voltage gain} = \frac{\text{Output voltage}}{\text{Differential input voltage}}$$

$$A = \frac{V_o}{V_{id}}$$

Because output signal amplitude is much large than the input signal the voltage gain is commonly called large signal voltage gain. For 741C is voltage gain is 200,000 typically.

11. Output voltage Swing:

The ac output compliance PP is the maximum unclipped peak to peak output voltage that an OPAMP can produce. Since the quiescent output is ideally zero, the ac output voltage can swing positive or negative. This also indicates the values of positive and negative saturation voltages of the OP-AMP. The output voltage never exceeds these limits for a given supply voltages +VCC and -VEE. For a 741C it is ± 13 V.

12. Output Resistance: (RO)

RO is the equivalent resistance that can be measured between the output terminal of the OPAMP and the ground. It is 75 ohm for the 741C OPAMP.

13. Output Short circuit Current :

In some applications, an OPAMP may drive a load resistance that is approximately zero. Even its output impedance is 75 ohm but cannot supply large currents. Since OPAMP is low power device and so its output current is limited. The 741C can supply a maximum short circuit output current of only 25mA.

14. Supply Current:

IS is the current drawn by the OP-AMP from the supply. For the 741C OPAMP the supply current is 2.8 m A.

15. Power Consumption:

Power consumption (PC) is the amount of quiescent power (Vin= 0V) that must be consumed by the OPAMP in order to operate properly. The amount of power consumed by the 741C is 85 m W.

16. Gain Bandwidth Product:

The gain bandwidth product is the bandwidth of the OPAMP when the open loop voltage gain is reduced to

1. From open loop gain vs frequency graph At 1 MHz shown in.fig.1.24,it can be found 1 MHz for the 741C OPAMP frequency the gain reduces to 1. The mid band voltage gain is 100, 000 and cut off frequency is 10Hz.

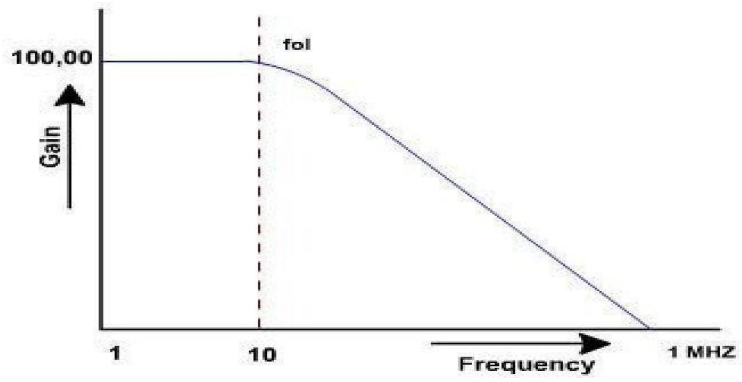


Fig 1.19: Band width of OP-AMP

17. Slew Rate: Slew rate is defined as the maximum rate of change of output voltage per unit **of time under large signal conditions and is expressed in volts / µsecs.**

To understand this, consider a charging current of a capacitor

$$i = C\frac{dV}{dt}$$

$$\frac{dV}{dt} = \frac{i}{C}$$

If 'i' is more, capacitor charges quickly. If 'i' is limited to Imax, then rate of change is also limited. Slew rate indicates how rapidly the output of an OP-AMP can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain and is normally specified at unity gain.

If the slope requirement is greater than the slew rate, then distortion occurs. For the 741C the slew rate is low 0.5 V / μS which limits its use in higher frequency applications.

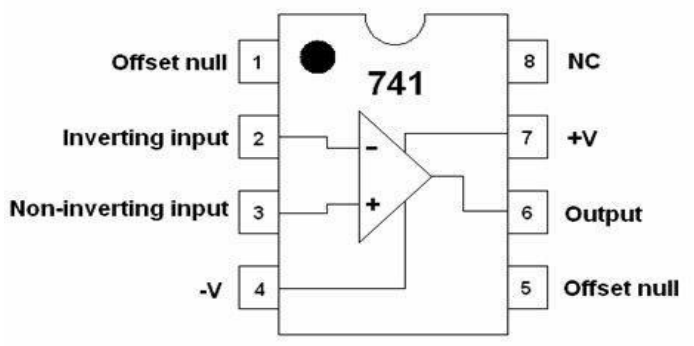
18. Input Offset Voltage and Current Drift:

It is also called average temperature coefficient of input offset voltage or input offset current. The input offset voltage drift is the ratio of the change in input offset voltage to change in temperature and expressed in ΔV /° C. Input offset voltage drift = (ΔVio /ΔT). Similarly, input offset current drift is the ratio of the change in input offset current to the change in temperature. Input offset current drift = (ΔIio / ΔT). For 741C,

ΔVio / ΔT = 0.5 V /

C. Iio/ ΔT = 12 pA / C

19. PIN DIAGRAM OF 741-OP AMP



FEATURES OF 741 OP-AMP:

1. No External frequency compensation is required

2. Short circuit Protection

3. Off Set Null Capability

4. Large Common mode and differential Voltage ranges

5. Low

6.

7.

8.

9.

10.

11.

12. Power Dissipation

13. No-Latch up Problem

7.741 is available in three packages:- 8-pin metal can, 10-pin flat pack and 8 or 14-pin DI.

1.10 MODES OF OPERATION OF OP-AMP

There are 2 modes in which an op-amp operates:

1.open loop mode

2.closed loop mode

Open loop OPAMP mode:

In the case of amplifiers the term open loop indicates that no connection exists between input and output terminals of any type. That is, the output signal is not fedback in any form as part of the input signal. In open loop configuration, The OPAMP functions as a high gain amplifier. There are three open loop OPAMP configurations.

1. The Differential Amplifier:

The open loop differential amplifier in which input signals vin1 and vin2 are applied to the positive and negative input terminals. Since the OPAMP amplifies the difference the between the two input signals, this configuration is called the differential amplifier. The

OPAMP amplifies both ac and dc input signals. The source resistance Rin1 and Rin2 are normally negligible compared to the input resistance Ri. Therefore voltage drop across these resistances can be assumed to be zero.

Therefore

v1 = vin1 and v2 = vin2. vo = Ad (vin1- vin2)

where, Ad is the open loop gain.

2. The Inverting Amplifier:

If the input is applied to only inverting terminal and non-inverting terminal is grounded then it is called inverting amplifier. This configuration is shown in fig 1.27.

v1= 0, v2 = vin. vo = -Ad vi

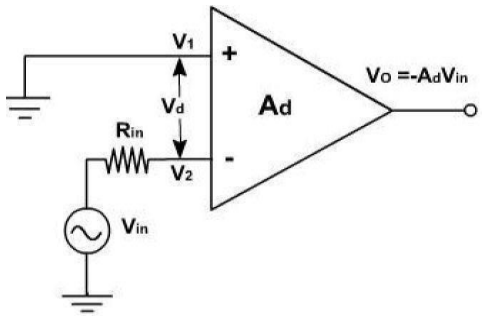


Fig 1.20: Inverting Amplifier

The negative sign indicates that the output voltage is out of phase with respect to input 180 ° or is of opposite polarity. Thus the input signal is amplified and inverted also.

3 .The non-inverting amplifier:

In this configuration, the input voltage is applied to non-inverting terminals and inverting terminal is ground as shown in fig.1.28

v1 = +vin , v2 = 0 vo = +Ad vin

This means that the input voltage is amplified by Ad and there is no phase reversal at the output.

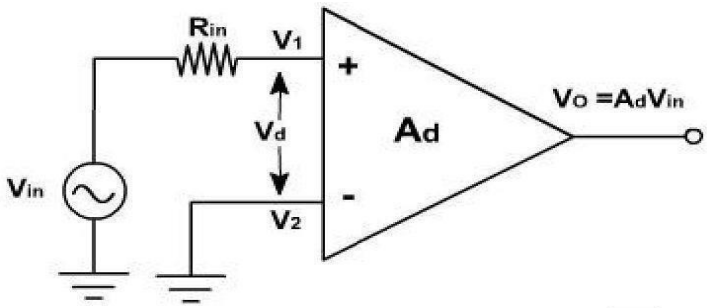


Fig 1.21: Non Inverting Amplifier

In all there configurations any input signal slightly greater than zero drive the output to saturation level. This is because of very high gain. Thus when operated in open-loop, the output of the OPAMP is either negative or positive saturation or switches between positive and negative saturation levels. Therefore open loop op-amp is not used in linear applications.

Closed Loop mode:

The Open Loop Gain of an ideal operational amplifier can be very high, as much as 1,000,000 (120dB) or more. However, this very high gain is of no real use to us as it makes the amplifier both unstable and hard to control as the smallest of input signals, just a few micro-**volts, (μV) would be enough to cause the output voltage to saturate and swing towards** one or the other of the voltage supply rails losing complete control of the output.

As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external Feedback Resistor called R***f***. **This** feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its Closed-loop Gain. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers bandwidth. This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a *Summing Point*. We must therefore separate the real input signal from the inverting input by using an Input Resistor, Rin. As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a *Virtual Earth* summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a "differential amplifier".

1.11 Inverting Amplifier Configuration

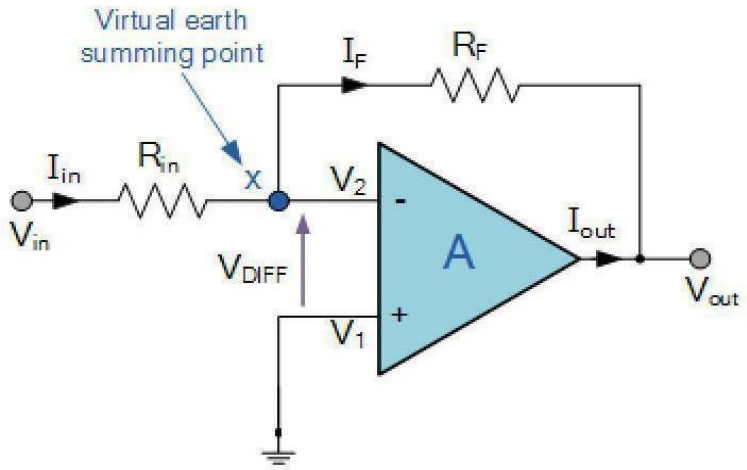


Fig 1.22: Inverting amplifier with feedback.

In this Inverting Amplifier circuit the operational amplifier is connected with feedback to produce a closed loop operation. For ideal op-amps there are two very important rules to remember about inverting amplifiers, these are: "no current flows into the input terminal" and that "V1 equals V2", (in real world op-amps both of these rules are broken). This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a "Virtual Earth". Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about Inverting Amplifiers or any operational amplifier for that matter and these are.

1. No Current Flows into the Input Terminals

2. The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.
Current (i) flows through the resistor network as shown.

$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

Then, the Closed-Loop Voltage Gain of an Inverting Amplifier is given as and this can be transposed to give Vout as:

$$V_{out} = -\frac{R_f}{R_{in}} * Vin$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180o out of phase. This is due to the feedback being negative in value.

1.12 The Non-inverting Amplifier

The second basic configuration of an operational amplifier circuit is that of a Non-inverting Amplifier. In this configuration, the input voltage signal, (Vin) is applied directly to the non- inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.
Feedback control of the non-inverting amplifier is achieved by applying a small part of the output voltage signal back to the inverting (- **) input terminal via a R*f*** - R2

divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and low output impedance, Rout as shown below.

Non-inverting Amplifier Configuration

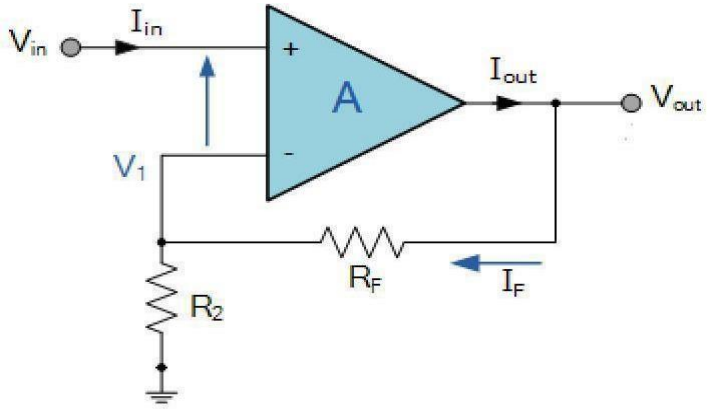


Fig 1.23: Non-inverting amplifier with feedback.

As said in the Inverting Amplifier that "no current flows into the input" of the amplifier and that "V1 equals V2". This was because the junction of the input and feedback signal (V1) are at the same potential. In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, R*f* and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and R*f* as shown below.

Equivalent Potential Divider Network

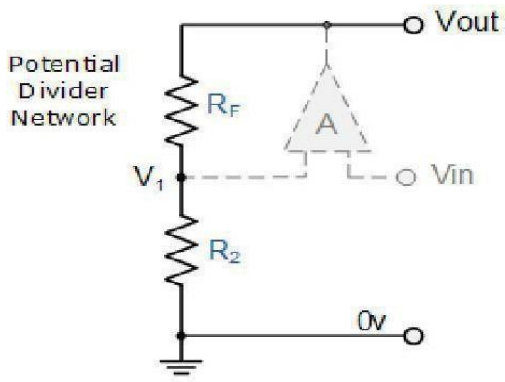


Fig 1.24: potential divider in non-inverting op-amp

From the fig 1.31 using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A V) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

Ideal Summing Point: $V_1 = V_{IN}$

Voltage Gain, $A_{(V)}$ is equal to: $\frac{V_{OUT}}{V_{IN}}$

Then, $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$

Transpose to give: $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$

We can see from the equation above, that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio **of the values of R*f* and R2. If the value of the feedback resistor R*f* is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor R2** is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, (Ao).

1.13 Voltage Follower (Unity Gain Buffer)

If we made the feedback resistor, R*f* equal to zero, (R*f* = 0), and resistor R2 equal to infinity, **(R2 = ∞) as shown in fig 1.32, then the circuit would have a fixed gain o**f "1" as all the output voltage would be present on the inverting input terminal (negative feedback). This would then produce a special type of the non-inverting amplifier circuit called a Voltage Follower or also called a "unity gain buffer".

As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, Vout = Vin. This then makes the voltage follower circuit ideal as a *Unity Gain Buffer* circuit because of its isolation properties as impedance or circuit isolation is more important than amplification while maintaining the signal voltage. The input impedance of the voltage **follower circuit is very high, typically above 1MΩ as it is** equal to that of the operational amplifiers input resistance times its gain (Rin x Ao). Also its output impedance is very low since an ideal op-amp condition is assume

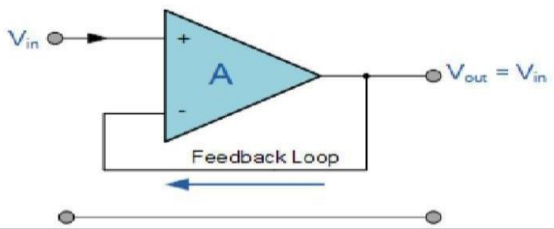


Fig 1.25: voltage follower

In this non-inverting circuit configuration, the input impedance Rin has increased to infinity and the feedback impedance Rf reduced to zero. The output is connected directly back to the negative inverting input so the feedback is 100% and Vin is exactly equal to Vout giving it a fixed gain of 1 or unity. As the input voltage Vin is applied to the non-inverting input the gain of the amplifier is given as:

$$V_{out} = A \times V_{in}$$

$$V_{in} = V + \; and \; V_{out} = V$$

One final thought, the output voltage gain of the voltage follower circuit with closed loop gain is **Unity**, the voltage gain of an ideal operational amplifier with open loop gain (no feedback) is **Infinite**. Then by carefully selecting the feedback components we can control the amount of gain produced by an operational amplifier anywhere from one to infinity.

1.13 INSTRUMENTATION AMPLIFIER:

In many industrial and consumer applications the measurement and control of physical conditions are very important. For example measurements of temperature and humidity inside a dairy or meat plant permit the operator to make necessary adjustments to maintain product quality. Similarly, precise temperature control of plastic furnace is needed to produce a particular type of plastic.

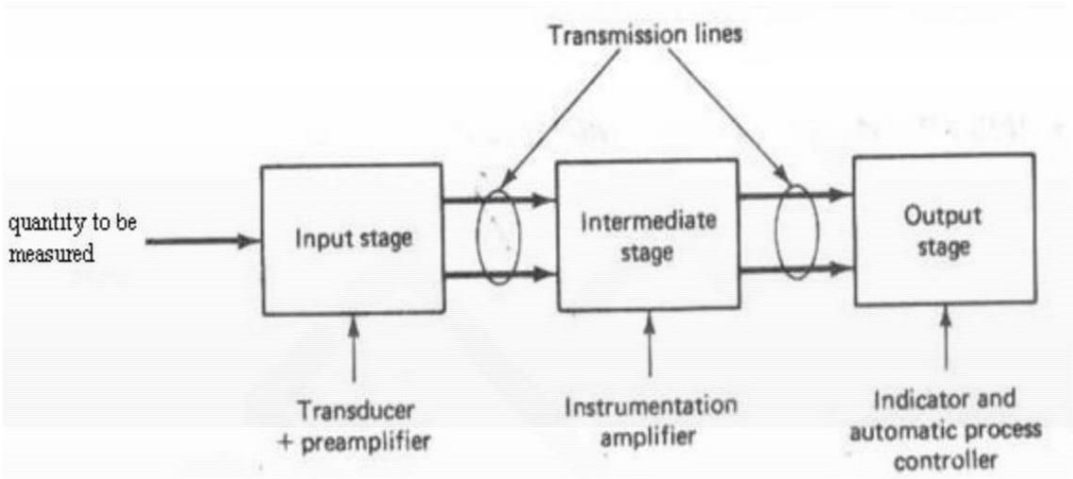


Fig.1.26: Instrumentation Amplifier

The transducer is a device that converts one form of energy into another. For example a strain gage when subjected to pressure or force undergoes a change in its resistance (electrical energy).An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it. Above fig shows a simplified form of such a system. The input stage is composed of a pre-amplifier and some sort of transducer, depending on the physical quantity to be measured. The output stage may use devices such as meters, oscilloscopes, charts, or magnetic records.

In Figure 1.33 the connecting lines between the blocks represent transmission lines, used especially when the transducer is at a remote test site monitoring hazardous conditions such as high temperatures or liquid levels of flammable chemicals. These transmission lines permit signal transfer from unit to unit. The length of the transmission lines depends primarily on the physical quantities tobe monitored and on system requirements.

The signal source of the instrumentation amplifier is the output of the transducer. Although some transducers produce outputs with sufficient strength to per- m.; their use directly, many do not. To amplify the low-level output signal of the transducer so that it can drive the indicator or display is the major function of the instrumentation amplifier.

Features of IA :

- **The instrumentation amplifier is intended for precise, low-level signal amplification where low noise, low thermal and time drifts.**
- **high input resistance.**
- **Accurate closed-loop gain are required.**
- **Low power consumption.**
- **high common-mode rejection ratio.**
- **High slew rate are desirable for superior performance.**

There are many instrumentation operational amplifiers, such as the /LA 725, ICL7605, and LH0036, that make a circuit extremely stable and accurate. These ICs are, however, relatively expensive; they are very precise special-purpose circuits in which most of the electrical parameters, such as offsets, drifts, and power consumption, are minimized,

whereas input resistance, CMRR, and supply range are optimized. Some instrumentation amplifiers are even available in modular form to suit special installation requirements.

Obviously, the requirements for instrumentation op-amps are more rigid than those for general-purpose applications. However, where the requirements are not too strict, the general-purpose op-amp can be employed in the differential mode.

We will call such amplifiers differential instrumentation amplifiers. Since most instrumentation systems use a transducer in a bridge circuit, we will consider a simplified differential instrumentation system arrangement using a transducer bridge circuit.

1.14 AC AMPLIFIER

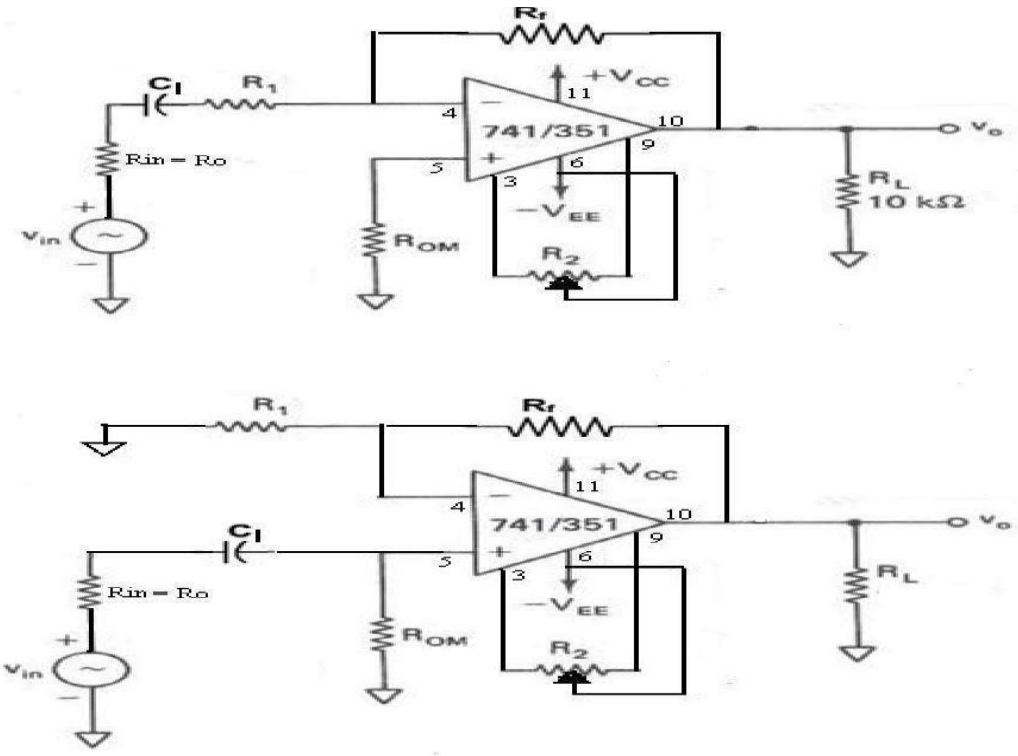


Fig 1.27: (a) AC Inverting Amplifier (b) AC Non Inverting Amplifier

1.15 V to I Converter:

Fig.1.35 shows a voltage to current converter in which load resistor R_L is floating (not connected to ground). The input voltage is applied to the non-inverting input terminal and the feedback voltage across R_1 drives the inverting input terminal. This circuit is also called a current series negative feedback amplifier because the feedback voltage across R_1 depends on the output current iL and is in series with the input difference voltage Vid. Writing the voltage equation for the input loop.

Vin = Vid + Vf

But Vid = 0 V , since A is very large, therefore,

Vin = Vf

vin = R* I_L

or I_L = V in / R.

and since input current is zero.

I_L = Iin = Vin ./ R

The value of load resistance does not appear in this equation.
Therefore, the output current is independent of the value of load resistance.
Thus the input voltage Vin is converted into output current I_L, the source must be capable of supplying this load current.

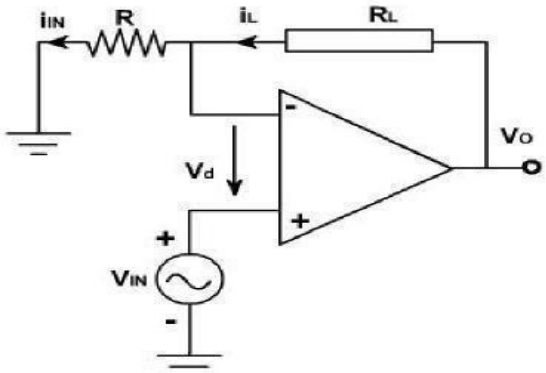


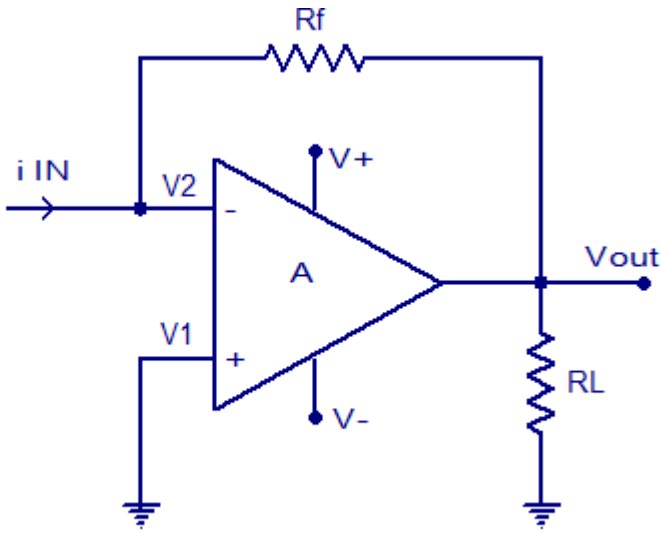
Fig 1.28: Circuit Diagram of V to I Converter

The maximum load current is VCC/ R. In this circuit Vin may be positive or negative.

1.16 I to V Converter:

Current to voltage converter:

The circuit shown in fig 1.36 is a current to voltage converter.



Active Transimpedance amplifer / current to voltage converter

Fig 1.29: Circuit Diagram of I to V Converter

Due to virtual ground the current through R is zero and the input current flows through Rf. Therefore, Vout = -Rf * Iin

The lower limit on current measure with this circuit is set by the bias current of the inverting input .

1.17 SAMPLE AND HOLD CIRCUITS:

The sample and hold circuit, as its name implies samples an i/p signal and holds on to it last sampled value until the i/p is sampled again. Below fig shows a sample and hold circuit using an op-amp with an E- MOSFET. In this circuit the E-MOSFET works as a switch that is controlled by the sample and control voltage Vs, and the capacitor C serves as a storage element.

The analog signal Vin to be sampled is applied to the drain, and sample and hold control voltage Vs is applied to the gate of the E-MOSFET. During the positive portion of the Vs, the EMOSFET conducts and acts as a closed switch. This allows i/p voltage to charge capacitor C. In other words input voltage appears across C and in turn at the o/p as shown in above fig.2.9.On the other hand, when Vs is zero, the EMOSFET is off and acts as open switch. The only discharge path for C is, through the op-amp. However the i/p resistance of the op-amp voltage follower is also very high; hence the voltage across C is retained.

The time periods Ts of the sample-and-hold control voltage Vs during which the voltage across the capacitor is equal to the i/p voltage are called sample periods. The time periods TH of Vs during which the voltage across the capacitor is constant are called hold periods. The o/p of the op-amp is usually processed/ observed during hold periods. To obtain the close approximation of the i/p waveform, the frequency of the sample-and-hold control voltage must be significantly higher than that of the i/p.

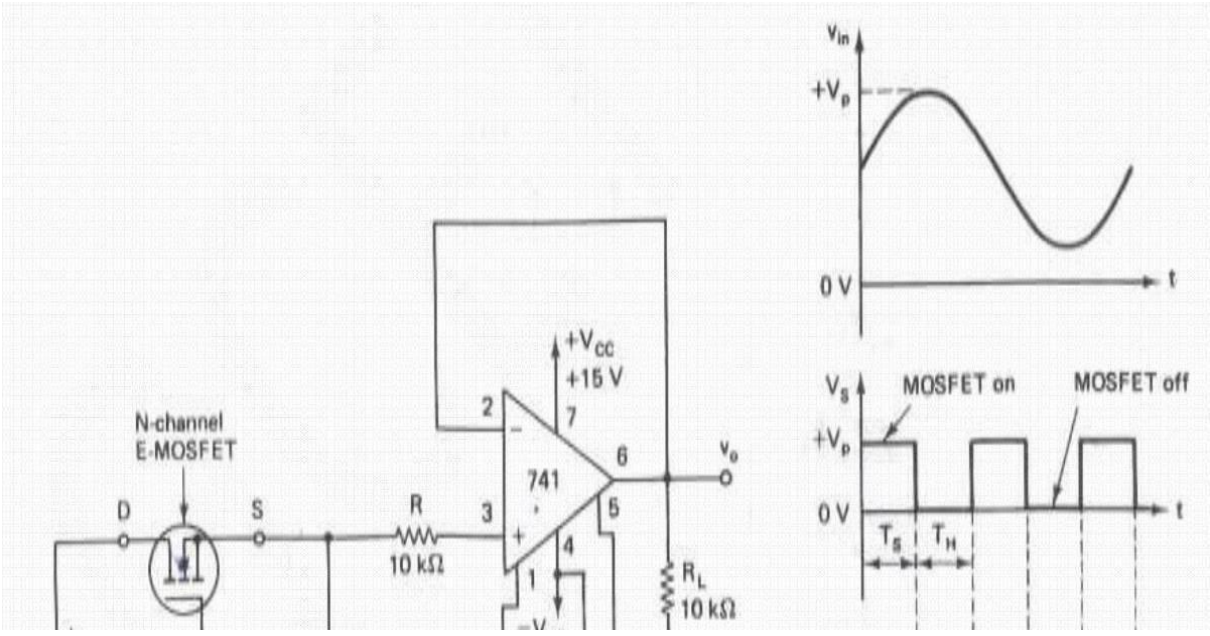


Fig.1.30: sample and hold circuit Fig 1.38 I/P and O/P wave forms

1.18 DIFFERENTIATOR:

A circuit in which the output voltage waveform is the differentiation of input voltage is called differentiator as shown infig.2.10.

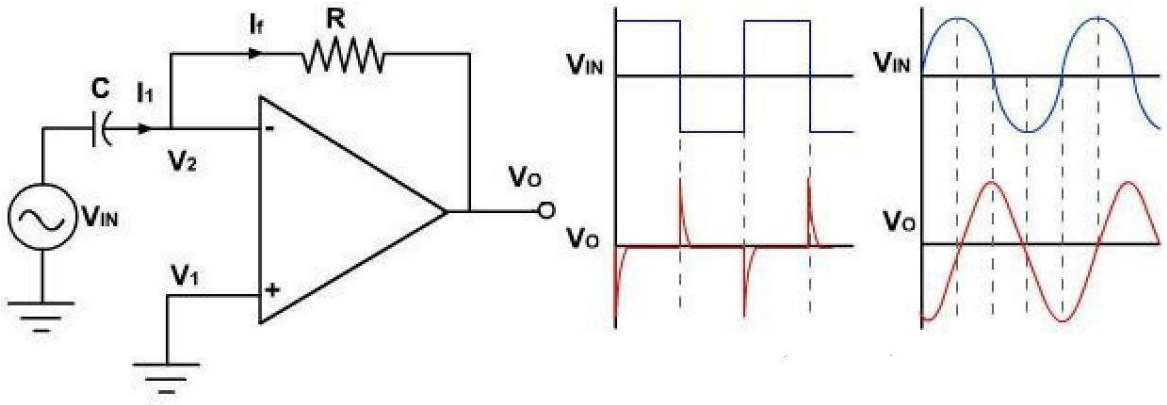


Fig.1.31: Circuit Diagram of Differentiator

The expression for the output voltage can be obtained from the Kirchoff's current equation written at node v2.

$$\text{Since,} \qquad i_{in} = i_f$$

$$\text{Therefore,} \quad C\frac{d}{dt}(V_{in} - 0) = \frac{0 - V_o}{R}$$

$$V_o = -RC\frac{dV_{in}}{dt}$$

Thus the output vo is equal to the RC times the negative instantaneous rate of change of the input voltage vin with time. A cosine wave input produces sine output. Fig.1.39 also shows the output waveform for different input voltages.

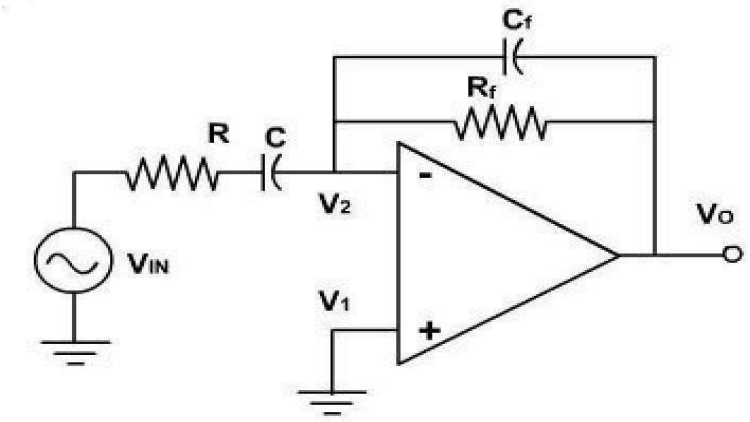


Fig.1.32: Circuit Diagram of Differentiator

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to Rf C. As the frequency changes, the gain changes. Also at higher frequencies the circuit is highly susceptible at high frequency noise and noise gets amplified. Both the high frequency noise and problem can be corrected by adding, few components. as shown in fig.1.40.

1.19 Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator. Fig.1.41**,** shows an integrator circuit using OPAMP.

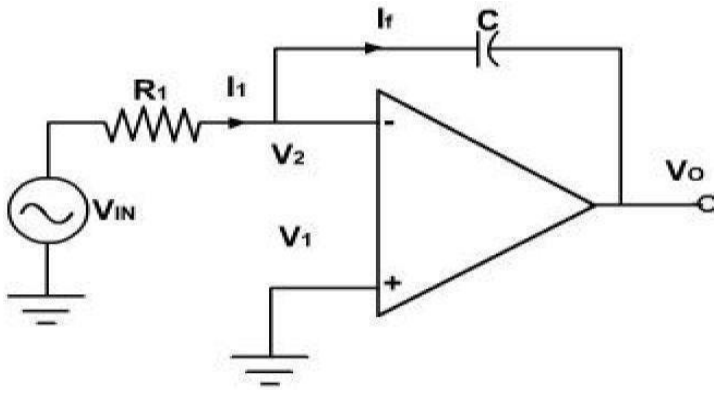


Fig.1.33: Circuit Diagram of Integrator

Here, the feedback element is a capacitor. The current drawn by OPAMP is zero and also the V2 is virtually grounded.

Therefore, i1 = if and v2 = v1 = 0

$$\frac{v_{in} - 0}{R} = C\,\frac{d(0 - v_o)}{dt}$$

Integrating both sides with respect to time from 0 to t, we get

$$\int_0^t \frac{v_{in}}{R}\,dt = \int_0^t C\frac{d(-v_o)}{dt}\,dt$$

$$= C(-v_o) + v_o\Big|_{t=0}$$

if $V_O|_{t=0} = 0$ V, then

$$v_o = \frac{-1}{R}\int_0^t v_{in}\,dt$$

The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC. If the input is a sine wave the output will be cosine wave. If the input is a square wave, the output will be a triangular wave. For accurate integration, the time period of the input signal T must be longer than or equal to RC.

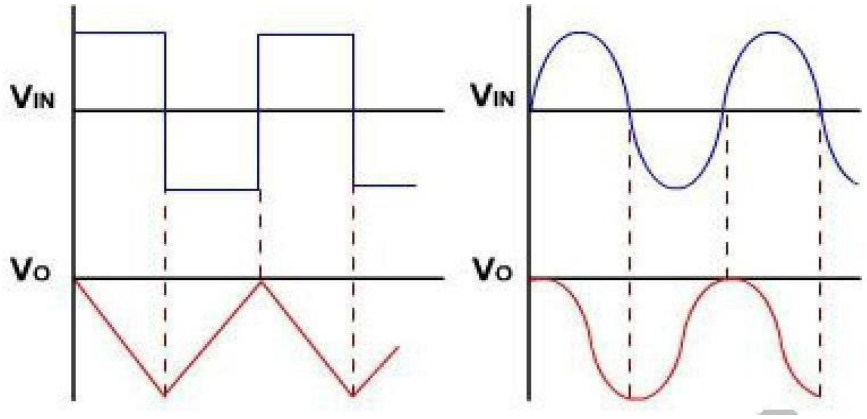


Fig 1.34: Input and Output wave forms

1.20 COMPARATOR:

Voltage comparator circuit:

Voltage comparator is a circuit which compares two voltages and switches the output to either high or low state depending upon which voltage is higher. A voltage comparator based on opamp is shown here. Fig2.14 shows a voltage comparator in inverting mode and Fig shows a voltage comparator in non inverting mode.

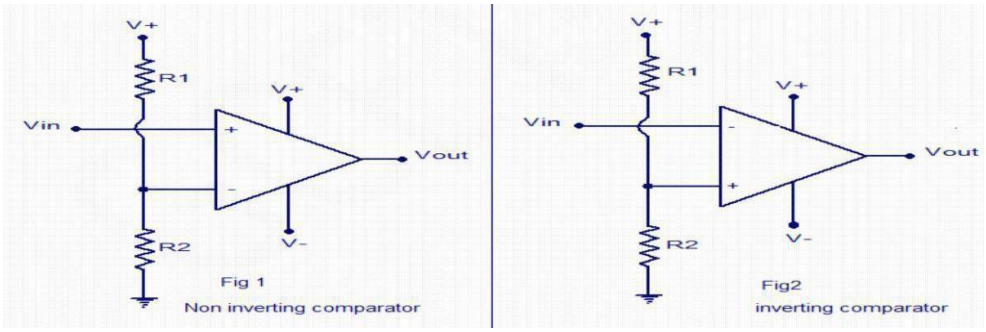


Fig 1.35: Circuit Diagram of Comparators **:**

In non inverting comparator the reference voltage is applied to the inverting input and the voltage to be compared is applied to the non inverting input. Whenever the voltage to be compared (Vin) goes above the reference voltage , the output of the opamp swings to positive

saturation (V+) and vice versa. Actually what happens is that, the difference between Vin and Vref, (Vin – Vref) will be a positive value and is amplified to infinity by the opamp. Since there is no feedback resistor Rf, the opamp is in open loop mode and so the voltage gain (Av) will be close to infinity. So the output voltage swings to the maximum possible value ie; V+. Remember the equation Av = 1 + (Rf/R1).

When the Vin goes below Vref, the reverse occurs.

Inverting comparator

In the case of an inverting comparator, the reference voltage is applied to the non inverting input and voltage to be compared is applied to the inverting input. Whenever the input voltage (Vin) goes above the Vref, the output of the op-amp swings to negative saturation. Here the difference between two voltages (Vin-Vref) is inverted and amplified to infinity by the op-amp. Remember the equation Av = - Rf/R1. The equation for voltage gain in the inverting mode is Av = - Rf/R1.Since there is no feedback resistor, the gain will be close to infinity and the output voltage will be as negative as possible i.e., V-.

Practical voltage comparator circuit.

A practical non inverting comparator based on uA741 opamp is shown below. Here the reference voltage is set using the voltage divider network comprising of R1 and R2. The equation is Vref = (V+/ (R1 + R2)) x R2. Substituting the values given in the circuit diagram into this equation gives Vref = 6V. Whenever Vin goes above 6V, the output swings to ~+12V DC and vice versa. The circuit is powered from a +/- 12V DC dual supply.

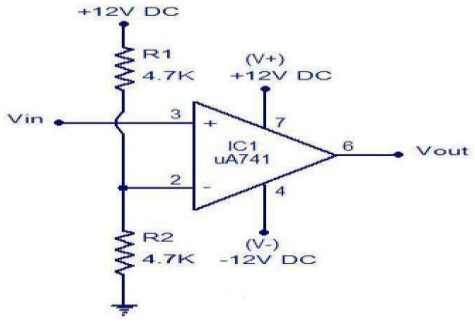
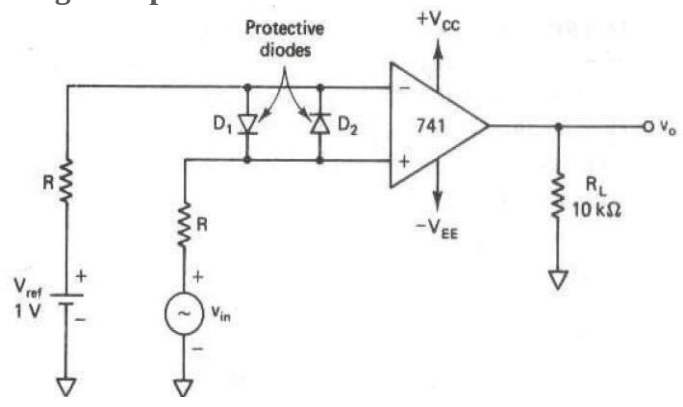


Fig 1.36: Circuit diagram of Practical voltage comparator.

Op-amp voltage comparator



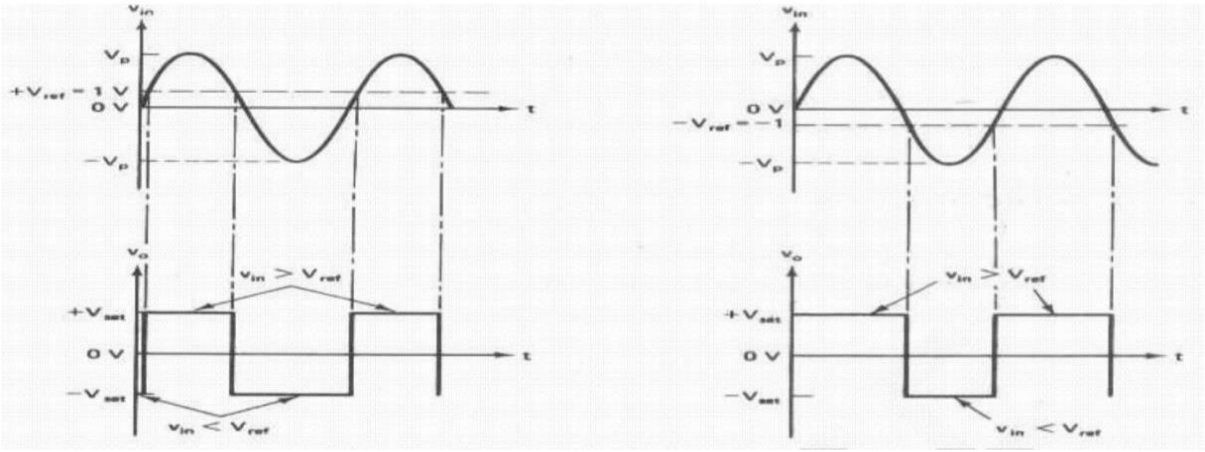


Fig 1.37: OP-AMP voltage comparator input and output waveforms (a,b,c)

1.21 SCHMITT TRIGGER:

Below fig shows an inverting comparator with +ve feed back. This circuit converts an irregular shaped wave forms to a square wave form or pulse. The circuit is known as schmitt trigger or squaring circuit. The i/p voltage being triggers the o/p Vo every time it exceeds certain voltage levels called the upper threshold voltage Vut and lower threshold voltage Vlt as shown in fig 1.45 (b).In fig 1.45 (a) these threshold voltages are obtained by using the voltage divider R1, R2, where the voltage across R1 is F/B to +ve i/p. The voltage across R1 is a variable reference, threshold voltage that depends on the value and polarity of the output voltage Vo. when Vo=+Vsat, the voltage across R1 is called the upper threshold voltage Vut.

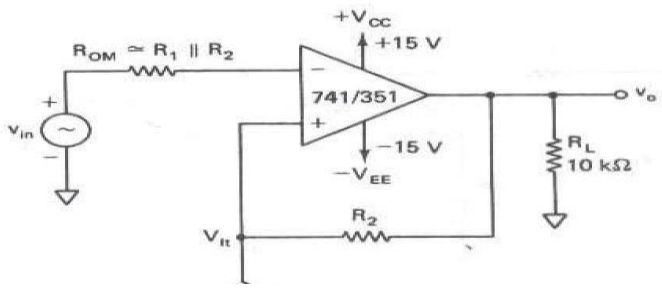


Fig 1.38 Schmitt Trigger

The input voltage Vin must be slightly more positive then Vut in order to cause the out put Vo to switch from +Vsat to –Vsat.as long as Vin less then Vut,Vo is at +Vsat. using the oltage divider rule, On the other hand,when Vo=-Vsat, the voltage across R1 is referred to as the lower

threshold voltage,Vlt.Vin must be slightly more negative than Vlt.in order to cause Vo to switch from-Vsat to +Vsat.in other words,for Vin values greater than Vlt,Vo is at – Vsat.Vlt is given by the following equation;

Thus if the threshold voltages Vut and Vlt are made large than the input noise voltages, the positive fed back will eliminate the false output transitions.Also the +ve feedback because of its regenerative action will make Vo switch faster between +Vsat and – Vsat.

1.22 MULTIVIBRATORS:

1.22.1 MONOSTABLE MULTIVIBRATOR:

The monostable multivibrator circuit using op-amp is shown in below figure1.47(a).The diode D1 is clamping diode connected across C the diode clamps the capacitor voltage to 0.7volts when the ouput is at +Vsat. A narrow –ve triggering pulse Vt is applied to the non-inverting input terminal through diode D2.

To understand the operation of the circuit,let us assume that the output Vo is at +Vsat that is **in it‘s stable state.** The diode D1 conducts and the voltage across the capacitor C that is Vc gets clamped to 0.7V.The voltage at the non-inverting input terminal is controlled by

potentiometric divider of R1R2 to βVo that is +βVsat in the stable state.

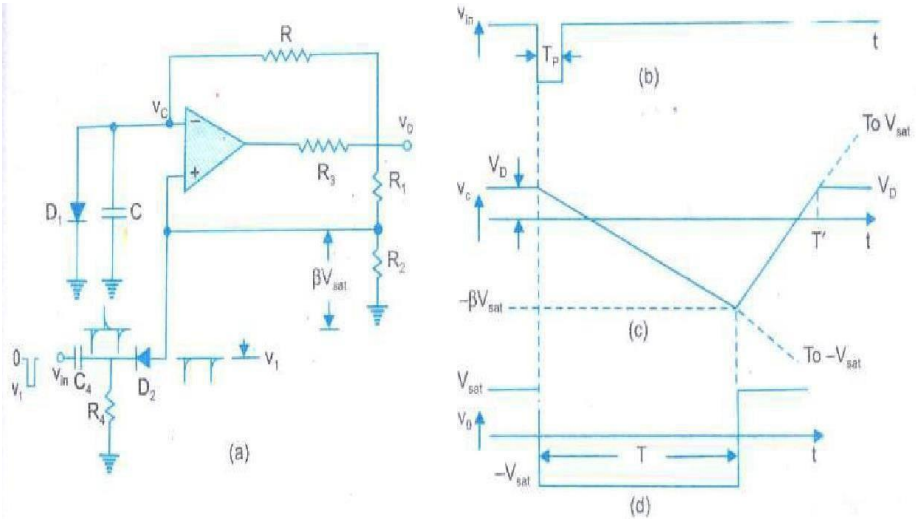


Figure1.39: Monostable Multivibrator and input-output waveforms (a,b,c,d)

Now if Vt ,a –ve trigger of amplitude Vt is applied to the non-inverting terminal, so that the effective voltage at this terminal is less than 0.7V than the output of th e op-amp **changes it's state from +Vsat to –**Vsat.The diode is now reverse biased and the capacitor starts charging exponentionally to –Vsat through the resistance R. The time constant of this

charging is r= RC.

1.23 INTRODUCTION TO VOLTAGE REGULATORS:

An unregulated power supply consists of a transformer (step down), a rectifier and a filter. These power supplies are not good for some applications where constant voltage is required irrespective of external disturbances. The main disturbances are:

1. As the load current varies, the output voltage also varies because of its poor regulation.

2. The dc output voltage varies directly with ac input supply. The input voltage may vary over a wide range thus dc voltage also changes.

3. The dc output voltage varies with the temperature if semiconductor devices are used.

An electronic voltage regulator is essentially a controller used along with unregulated power supply to stabilize the output dc voltage against three major disturbances

a. Load current (IL)

b. Supply voltage (Vi)

c. Temperature (T)

Fig.1.48, shows the basic block diagram of voltage regulator.

where Vi = unregulated dc voltage. Vo = regulated dc voltage.

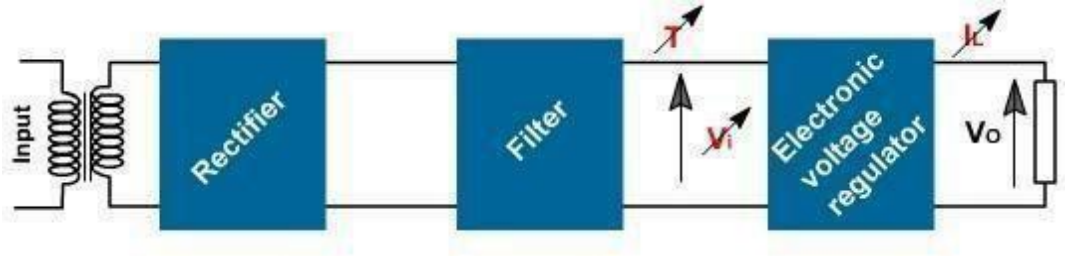


Fig.1.40: Block Diagram of voltage regulator

Since the output dc voltage VLo depends on the input unregulated dc voltage Vi, load current

IL and the temperature t, then the change ΔVo in output voltage of a power supply can be

expressed as follows

$$VO = VO (Vi, IL, T)$$

Take partial derivative of VO, we get,

$$VO = VO(Vi, IL, T)$$

Take partial derivative of VO, we get,

$$\Delta V_O \frac{\partial V_O}{\partial V_i}\Delta Vi + \frac{\partial V_O}{\partial IL}\Delta I_L + \frac{\partial V_O}{\partial T}\Delta T$$

or

$$\Delta V_O = S_V \Delta V_i + R_L \Delta I_L + S_T \Delta T$$

$$S_V = \frac{\Delta V_O}{\Delta V_i}\Big|_{\substack{\Delta I_L=0 \\ \Delta T=0}}$$

$$R_O = \frac{\Delta V_O}{\Delta I_L}\Big|_{\substack{\Delta V_i=0 \\ \Delta T=0}}$$

$$S_T = \frac{\Delta V_O}{\Delta T}\Big|_{\substack{\Delta V_i=0 \\ \Delta IL=0}}$$

SV gives variation in output voltage only due to unregulated dc voltage. RO gives the output voltage variation only due to load current. ST gives the variation in output voltage only due to temperature.

The smaller the value of the three coefficients, the better the regulations of power supply. The input voltage variation is either due to input supply fluctuations or presence of ripples due to inadequate filtering. A voltage regulator is a device designed to maintain the output voltage of power supply nearly constant. It can be regarded as a closed loop system because it monitors the output voltage and generates the control signal to increase or decrease the supply voltage as necessary to compensate for any change in the output voltage. Thus the purpose of voltage regulator is to eliminate any output voltage variation that might occur because of changes in load, changes in supply voltage or changes in temperature.

Zener Voltage Regulator:

The regulated power supply may use zener diode as the voltage controlling device as shown in fig.1.49. The output voltage is determined by the reverse breakdown voltage of the zener diode. This is nearly constant for a wide range of currents. The load voltage can bemaintained constant by controlling the current through zener.

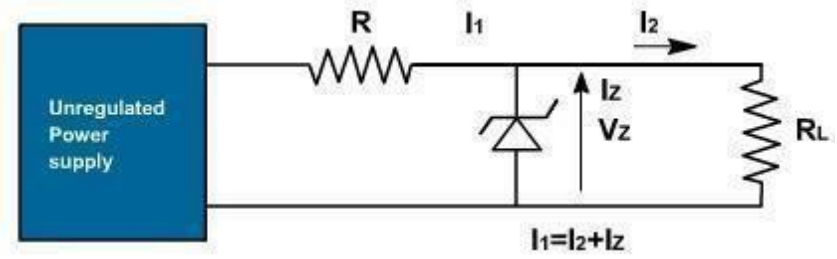


Fig.1.41: Circuit diagram of Zener voltage regulator

The zener diode regulator has limitations of range. The load current range for which regulation is maintained, is the difference between maximum allowable zener current and minimum current required for the zener to operate in breakdown region. For example, if zener diode requires a minimum current of 10 mA and is limited to a maximum of 1A (to prevent excessive dissipation), the range is 1 - 0.01 = 0.99A. If the load current variation exceeds 0.99A, regulation may be lost.

Emitter Follower Regulator:

To obtain better voltage regulation in shunt regulator, the zener diode can be connected to the base circuit of a power transistor as shown in fig.1.50. This amplifies the zener current range. It is also known as emitter follower regulation.

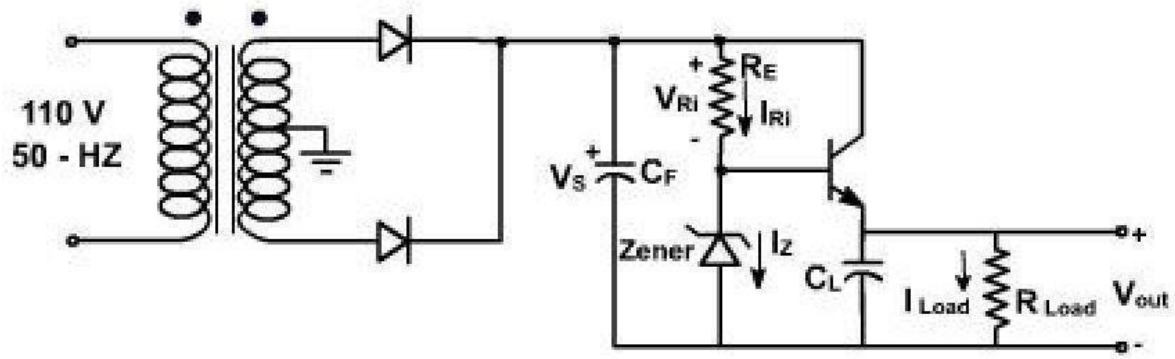


Fig. 1.42: Circuit diagram of Emitter follower voltage regulator

This configuration reduces the current flow in the diode. The power transistor used in this configuration is known as pass transistor. The purpose of CL is to ensure that the variations in one of the regulated power supply loads will not be fed to other loads. That is the capacitor effectively shorts out high frequency variations.Because of the currents amplifying property of the transistor, the current in the zenor dioide is small. Hence there is little voltage drop across the diode resistance, and the zener approximates an ideal constant voltage source.

Operation of the circuit:

The current through resistor R is the sum of zener current IZ and the transistor base current **IB(= IL / β).**

$$IL = IZ + IB$$

The output voltage across RL resistance is given by VO = VZ - VBE
Where VBE =0.7 V

Therefore, VO= constant.

The current IR is assumed to be constant for a given supply voltage. Therefore, if IL increases, it needs more base currents, to increase base current Iz decreases. The difference in this regulator with zener regulator is that in later case the zener current decreases (increase) by same amount by which the load current increases (decreases). Thus the current range is less, while in the shunt regulators, if IL

increases by ΔIL then IB should increase by ΔIL / β or IZ should decrease by ΔIL / β.

Therefore the current range control is more for the same rating zener.

IC package should be secured to a heat sink. When this is done, ILoad can increase to about 1.5 A. We now focus our attention on the 78XX series of regulators. The last two digits of the IC par number denote the output voltage of the device. Thus, for example, a 7808 IC
The current through resistor R is the sum of zener current IZ and the transistor
base current **IB(= IL / β).**

IL = IZ + IB

The output voltage across RL resistance is given by VO = VZ - VBE

Where VBE =0.7 V

Therefore, VO= constant.

The emitter current is same as load current. The current IR is assumed to be constant for a given supply voltage. Therefore, if IL increases, it needs more base currents, to increase base current Iz decreases. The difference in this regulator with zener regulator is that in later case the zener current decreases (increase) by same amount by which the load current increases (decreases). Thus the current range is less, while in the shunt regulators, if IL

increases by ΔIL then IB should increase by ΔIL / β or IZ should decrease by ΔIL / β.

Therefore the current range control is more for the same rating zener.

IC package should be secured to a heat sink. When this is done, ILoad can increase to about 1.5 A. We now focus our attention on the 78XX series of regulators. The last two digits of the IC par number denote the output voltage of the device. Thus, for example, a 7808 IC
package produces a 8V regulated output. These packages, although internally complex, are inexpensive and easy to use.

There are a number of different voltages that can be obtained from the 78XX series 1C; they are 5, 6, 8, 8.5, 10, 12, 15, 18, and 24 V. In order to design a regulator around one of these ICs, we need only select a transformer, diodes, and filter.

1. Input and output short circuit protection provided.

2. Positive or negative supply operation

3. Good line and load regulation

4. Low temperature drift and high ripple rejection

5. Output voltage can be varied from 2V to 37V

6. Small in size and hence economical.

UNIT-III

3.1 LOW PASS FILTER:

- An electric filter is often a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filters may be classified in a number of ways:

1. **Analog or digital**
2. **Passive or active**
3. **Audio (AF) or radio frequency (RF)**

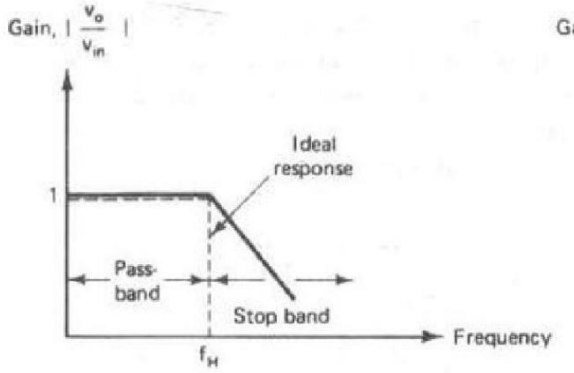
- Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques.
- Depending on the type of elements used in their construction, filters maybe classified as passive or active.
- Elements used in passive filters are resistors, capacitors, and inductors.
- Active filters, on the other hand, employ transistors or op-amps in addition to the resistors and capacitors.
- The type of element used dictates the operating frequency range of the filter.
- For example, RC filters are commonly used for audio or low-frequency operation, whereas
- LC or crystal filters are employed at RF or high frequencies. Especially because of their high Q value (figure of merit),
- the crystal provide more stable operation at higher frequencies.
- **An active filter offers the following advantages over a passive filter:**

1. Gain and frequency adjustment flexibility: Since the op-amp is capable of providing again, the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.

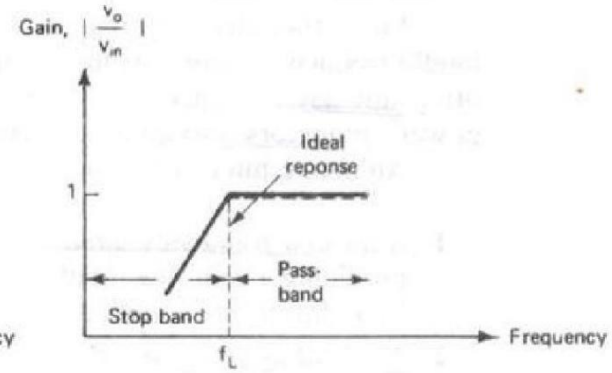
2. No loading prob1em: Because of the high input resistance and low output resistance of the op-amp, the active filter does not cause loading of the source or load.

3. Cost: Typically, active filters are more economical than passive filters. This is because of the variety of cheaper op-amps and the absence of inductors. The most commonly used filters are these:

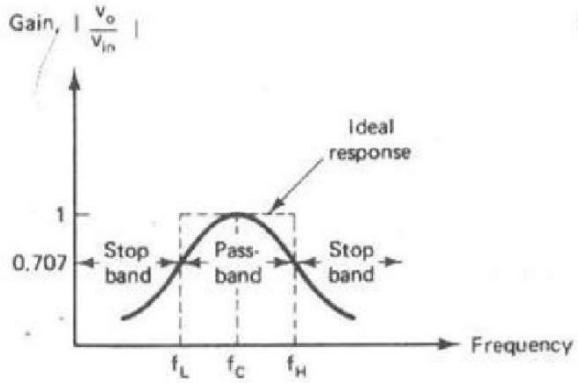
1. **Low-pass filter**
2. **High-pass filter**
3. **Band-pass filter**
4. **Band-reject filter**
5. **All-pass filter**


Gain, $\left|\frac{V_o}{V_{in}}\right|$
Ideal response
1
Pass-band
Stop band
Frequency
f_H

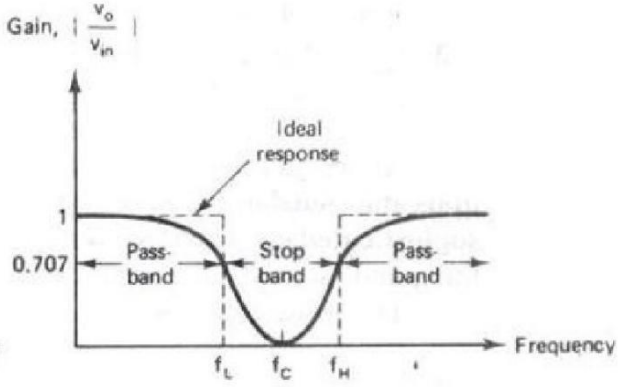
(a)


Gain, $\left|\frac{V_o}{V_{in}}\right|$
Ideal reponse
1
Stop band
Pass-band
Frequency
f_L

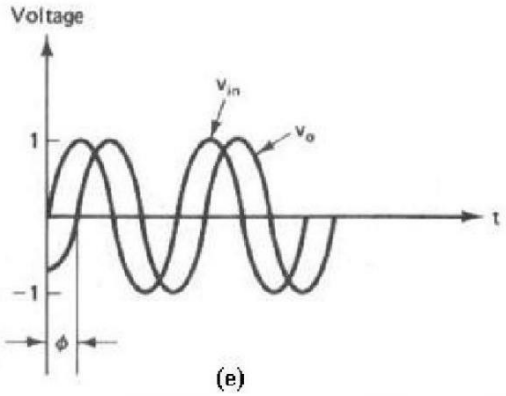
(b)


Gain, $\left|\frac{V_o}{V_{in}}\right|$
Ideal response
1
0.707
Stop band
Pass-band
Stop band
Frequency
f_L
f_C
f_H

(c)


Gain, $\left|\frac{V_o}{V_{in}}\right|$
Ideal response
1
0.707
Pass-band
Stop band
Pass-band
Frequency
f_L
f_C
f_H

(d)


Voltage
V_{in}
V_o
1
-1
t
ϕ

(e)

Fig 3.1: Frequency response of major active filters (a) Low pass (b)

High pass (c) Band pass (d) Band reject (e) All pass

- Fig.3.1 shows the frequency response characteristics of the five types of filters. The ideal response is shown by dashed curves, while the solid lines indicate the practical filter response.
- A low-pass filter has a constant gain from 0Hz to a high cut-off frequency fH. Therefore, the bandwidth is also fH. At fH the gain is down by 3dB; after that (f>fH) it decreases with the increase in input frequency. The frequencies between 0 Hz and fH are known as the pass band frequencies, whereas the range of frequencies, those beyond fH that are attenuated includes the stop band frequencies.

- Fig.3.1 (a) shows the frequency response of the low-pass filter. As indicated by the dashed line, an ideal filter has a zero loss in its pass band and infinite loss in its stop band. Unfortunately, ideal filter response is not practical because linear networks cannot produce the discontinuities. However, it is possible to obtain a practical response that approximates the ideal response by using special design techniques, as well as precision component values and high-speed op-amps.
- Butterworth, Chebyshev, and Cauer filters are some of the most commonly used practical filters that approximate the ideal response.
- The key characteristic of the Butterworth filter is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat-flat filter. The Chebyshev filter has a ripple pass band and flat stop band i.e. the Cauer filter has a ripple pass band and a ripple stop band.

Generally, the Cauer filter gives the best stop band response among the three. Because of their simplicity of design, the low-pass and high-pass Butterworth filters are discussed here.

- Figure3 -1(b) shows a high-pass filter with a stop band 0<f<fL and a pass band f>fL. fL is the low cutoff frequency, and is the operating frequency.
- A band-pass filter has a pass band between two cut off frequencies fH and fL, where fH>fL and two stop-bands: 0<f<fL and f>fH. The bandwidth of the band- pass filter, therefore, is equal to fH-fL.
- The band-reject filter performs exactly opposite to the band-pass; that is, it has a band-stop between two cutoff frequencies fH and fL and two pass bands: 0<f<fL and f>fH. The band-reject is also called a band-stop or band-elimination filter. The frequency responses of band- pass and band-reject filters are shown in Figure (c) and (d), respectively. In these figures, fC is called the center frequency since it is approximately at the center of the pass band or stop band.Fig.1 (e) shows the phase shift between input and output voltages of an all-pass filter.

This filter passes all frequencies equally well; that is, output and input voltages equal in amplitude for all frequencies, with the phase shift between the two a function of frequency. The highest frequency up to which the input and output amplitudes remain equal is dependent on the unity gain bandwidth of the op-amp. (At this frequency, however, the phase shift between the input and output is maximum.

The rate at which the gain of the filter changes in the stop band is determined by the order of the filter. For example, for the first order low-pass filter the gain-rolls-off at the rate of 20dB/decade in the stop band, that is, for f>fH; on the other hand, for the second-order low-pass filter the roll-off rate is 40dB/decade and soon. By contrast, for the first-order high

pass filter the gain increases at the rate of 20 dB/decade in the stop band, that is, until f=fL;

the increase is 40dB/decade for the second-order high-pass filter;

3.1.1 FIRST-ORDER LOW-PASSBUTTER WORTH FILTER

Fig. shows a first-order low-pass Butterworth filter that uses an RC network for filtering. Note that the op- amp is used in the non-inverting configuration; hence it does not load down the RC network. ResistorsR1 and RF determine the gain of the filter. According to the voltage-divider rule, the voltage at the non-inverting terminal (across capacitor C) is

$$V_1 = \frac{-jX_C}{R - jX_C} V_{in}$$

$$j = \sqrt{-1} \; and - jX_C = \frac{1}{j2\pi fC}$$

$$V_1 = \frac{V_{in}}{1 + j2\pi fRC}$$

$$V_o = 1 + \frac{R_F}{R_1} V_1$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) \frac{V_{in}}{1 + j2\pi fRC}$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j\left(f / f_H\right)}$$

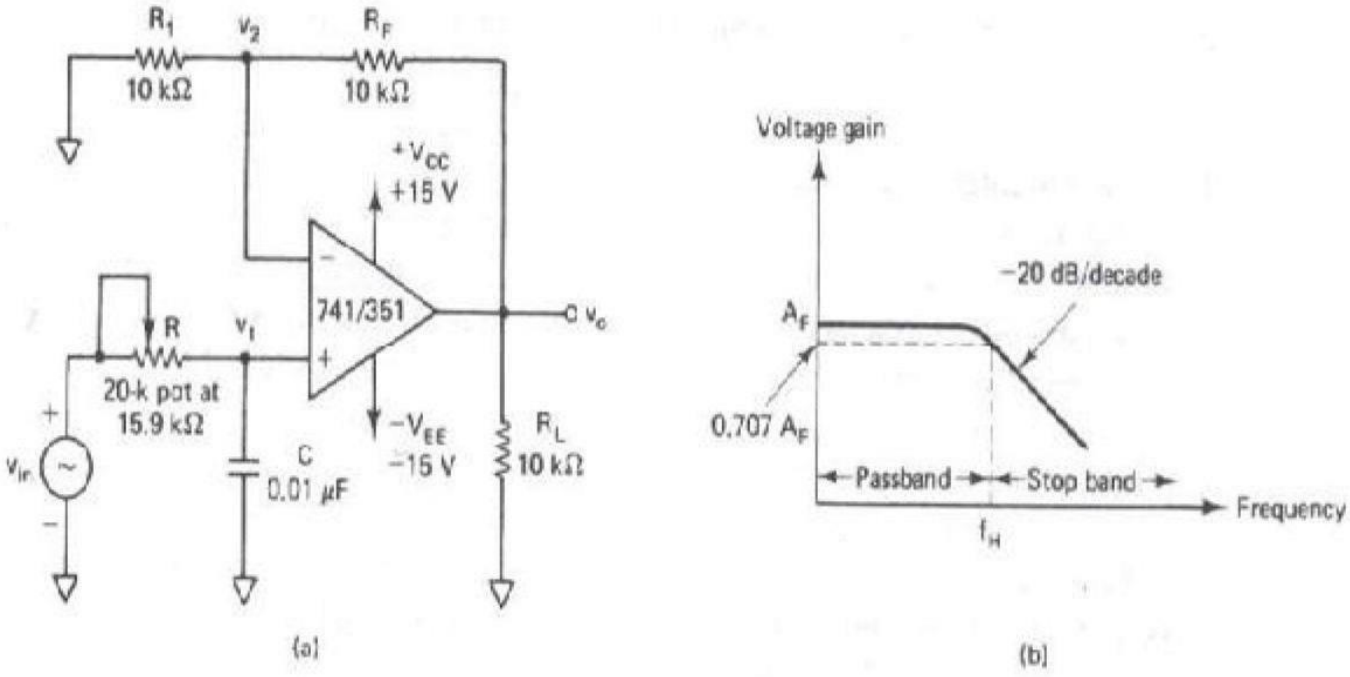


Fig 3.2: First order Low Pass Butter Worth Filter (a) circuit (b) Response

Where Vo/Vin =gain of the filter as a function of frequency

$A_F = \left(1 + \frac{R_F}{R_1}\right)$

= pass band gain of the filter

f = input frequency of the filter

$f_H = \frac{1}{2\pi RC}$ = upper cut-off frequency of the filter.

The gain magnitude and phase angle equations of the low-pass filter can be obtained by converting Equation 3.1into its equivalent polar form, as follows:

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + (f/f_H)^2}}$$

$$\Phi = -tan^{-1}\left(\frac{f}{f_H}\right)$$

Where **φ is the phase angle in degrees.**

The operation of the low pass filter can be verified from the gain magnitude equation:

1. At very low frequencies that is , f<fH, $\left|\frac{V_o}{V_{in}}\right| = A_F$
2. At f=fH, $\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\ A_F$
3. At f>fH , $\left|\frac{V_o}{V_{in}}\right| < A_F$

3.1.2 Filter Design

A low-pass filter can be designed by implementing the following steps:

1. Choose a value of high cutoff frequency *fH*.

2. Select a value of C less than or equal to 1 μF. Mylar or tantalum capacitors are

recommended for better performance.

3. Calculate the value of R using R = $\frac{1}{2\pi f_H C}$

4. Finally, select values of R1 and RF dependent on the desired pass band gain AF using

$A_F = 1 + \frac{R_f}{R_1}$

3.1.3 Frequency Scaling

Once a filter designed; there may sometimes be a need to change its cut-off frequency. The procedure used to convert an original cut-off frequency *fH* to a new cut-off frequency ***f'H*** is called frequency scaling. Frequency scaling is accomplished as follows. To change a high cutoff frequency, multiple R or C, but not both, by the ratio of the original cutoff frequency to the new cutoff frequency.

3.1.4 SECOND-ORDER LOW-PASSBUTTER WORTH FILTER

A stop-band response having a 40-dB/decade roll-off is obtained with the second order low-pass filter. A first-order low-pass filter can be converted into a second order type simply by using an additional RC network, as shown in Fig.3.3.

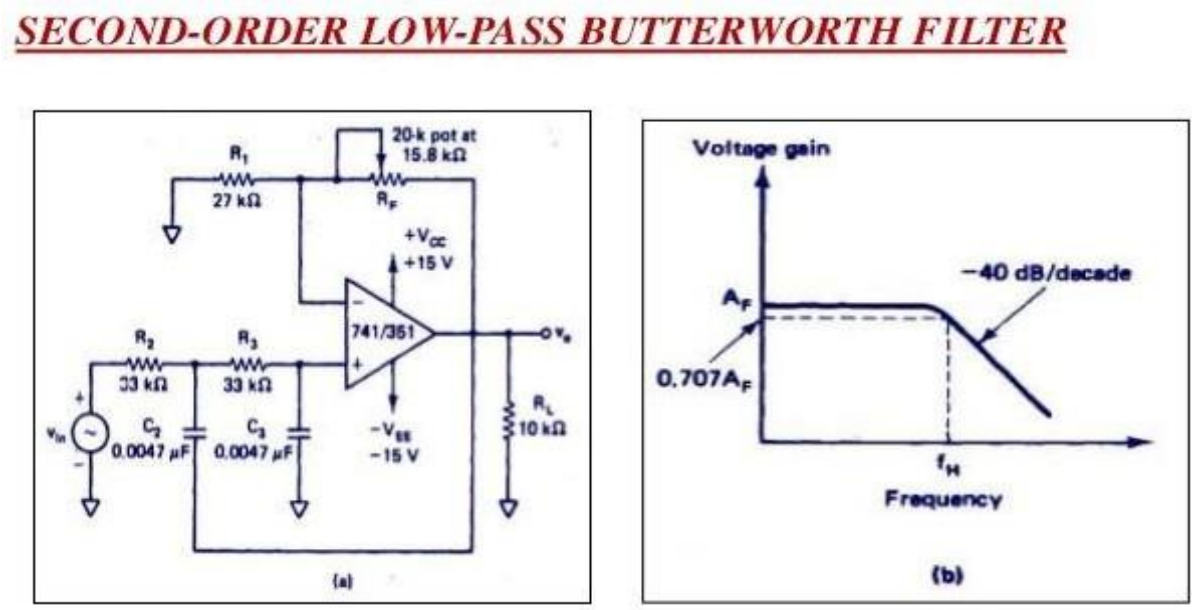


Fig 3.3: Second order Low Pass Butter Worth Filter a)Circuit(b)Frequency Response

Second-order filters are important because higher-order filters can be designed using them. The gain of the second-order filter is set by R1 and RF, while the high cutoff frequency fH is determined by R2, C2, R3, and C3, as follows

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

Furthermore, for a second-order low-pass Butterworth response, the voltage gain magnitude equation is

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$$

Where Vo/Vin = gain of the filter as a function of frequency

$A_F = \left(1+\frac{R_F}{R_1}\right)$ = pass band gain of the filter

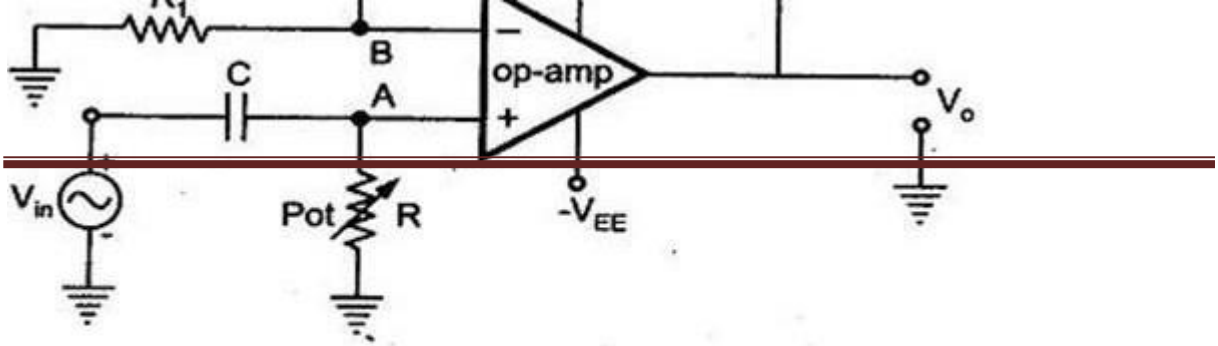


FIG FIRST ORDER HIGH PASS BUTTER WORTH FILTER

3.2 HIGH PASS FILTER

3.2.1 FIRST-ORDER HIGH-PASSBUITERWORTH FILTER

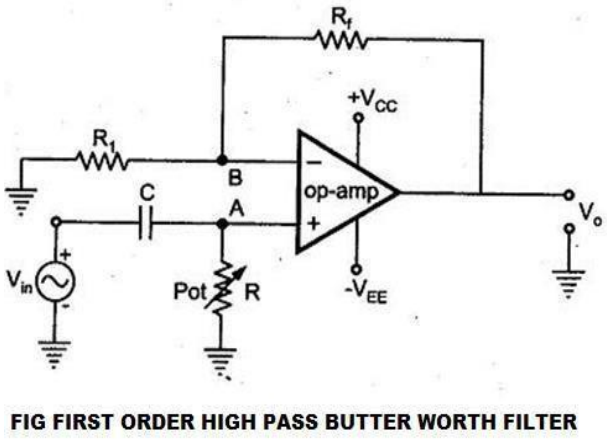
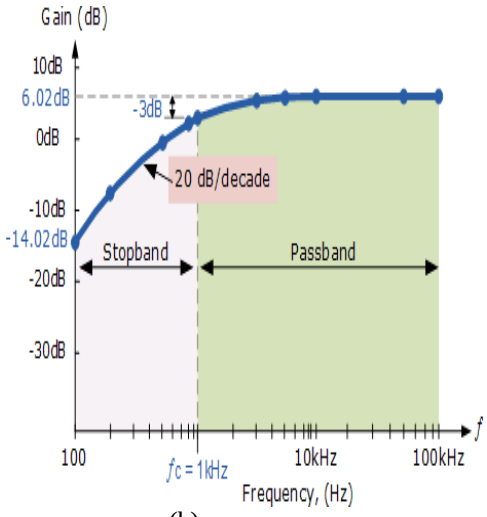


FIG FIRST ORDER HIGH PASS BUTTER WORTH FILTER

(a)



(b)

Fig 3.5: (a) First order High Pass Butter worth Filter (b) Frequency Response High-pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters. That is, a first-order high-pass filter is formed from a first-order low-pass type by interchanging components Rand C.

Similarly, a second-order high-pass filter is obtained from a second-order low-pass filter if R and Care interchanged, and so on. Figure3.4 shows a first-order high-pass Butterworth filter with a low cutoff frequency of fL.

This is the frequency at which the magnitude of the gain is 0.707 times its pass band value. Obviously,
All frequencies higher than *fL* are pass-band frequencies, with the highest frequency determined by the closed- loop bandwidth of the op-amp.

Note that the high-pass filter of Figure 3.4(a) and the low-pass filter of Figure3.4(a) are the same circuits, except that the frequency-determining components(R and C) are interchanged. For the first-order high-pass filter of Figure 3.4(a), the output voltage is

$$V_o = \left(1 + \frac{R_f}{R_1}\right)\frac{j2\pi fRC}{1 + j2\pi fRC}V_{in}$$

$$\frac{V_o}{V_{in}} = A_F\frac{j(f/f_L)}{\sqrt{1 + j(f/f_L)}}$$

Hence the magnitude of the voltage gain is

$$\left|\frac{V_o}{V_{in}}\right| = A_F\frac{(f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

3.3 BAND-PASS FILTERS

A band-pass filter has a pass band between two cutoff frequencies *fH* and fL such that *fH>fL*. Any input frequency outside this pass band is attenuated. Basically, there are two types of band-pass filters:

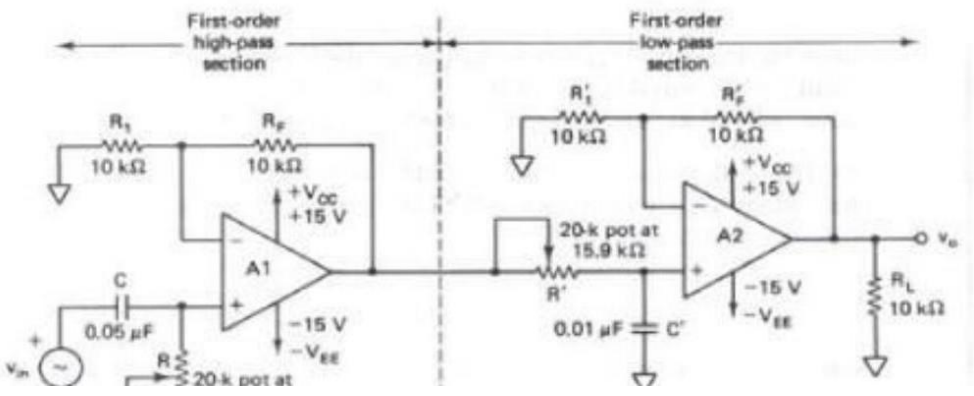
(1) Wide band pass, and

(2) Narrow band pass.

Unfortunately, there is no set dividing line between the two. However, we will define a filter as wideband pass if its figure of merit or quality factor Q<10.On the other hand, if we will call the filter a narrow band-pass filter. Thus Q is a measure of selectivity, meaning the higher the value Q, the more selective is the filter or the narrower its bandwidth (BW). The relationship between Q, the3- dB bandwidth, and the center frequency fc is given by For the wideband-pass filter the center frequency *fc* can be defined as where *fH* =high cut off frequency(Hz) *fL*=low cut off frequency of the wideband-pass filter (Hz) In a narrowband-pass filter, the output voltage peaks at the center frequency.

3.3.1 Wide-band pass filter

A wide band-pass filter can be formed by simply cascading high-pass and low-pass sections and is generally the choice for simplicity of design and performance. To obtain ±20dB/decade band-pass, first-order high pass and first order low-pass sections are cascaded; fora±40-dB/decade band-pass filter, second-order high- pass and second-order low-pass sections are connected in series. Figure3. 6 showsthe±20-dB/decade wideband pass filter, which is composed of first-order high- pass and first-order low-pass filters. To realize a band-pass response, however, fH must be larger than *fL*.



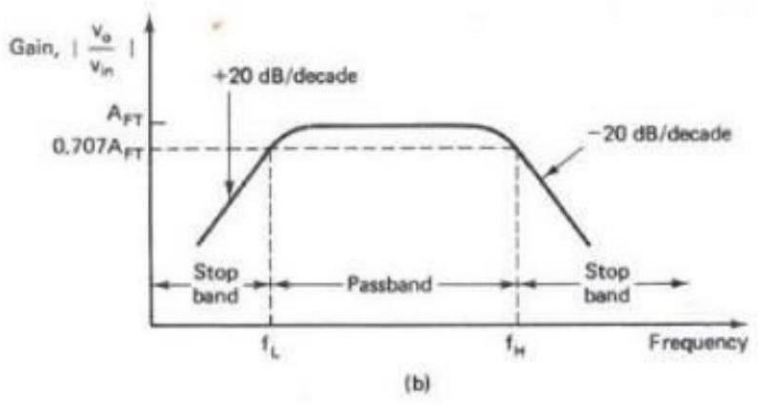


Fig 3.6(a)±20dB/decade Wide Band Pass Filter (b)Frequency Response

Since the band-pass gain is 4, the gain of the high-pass as well as low-pass sections could be set equal to 2. That is, input and feedback resistors must be equal in **value, say10 kΩ** each. The complete band-pass filter is shown in Fig 3.6(a).(b)The voltage gain magnitude of the band-pass filter is equal to the product of the voltage gain magnitudes of the high-pass and low-pass filters.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F(f/f_L)}{\sqrt{1+(f/f_L)^2}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}(f/f_L)}{\sqrt{[1+(f/f_L)^2][1+(f/f_H)^2]}}$$

Where *AFT* =total pass band gain

f= frequency of the input signal (Hz)

fL=low cut off frequency(Hz)

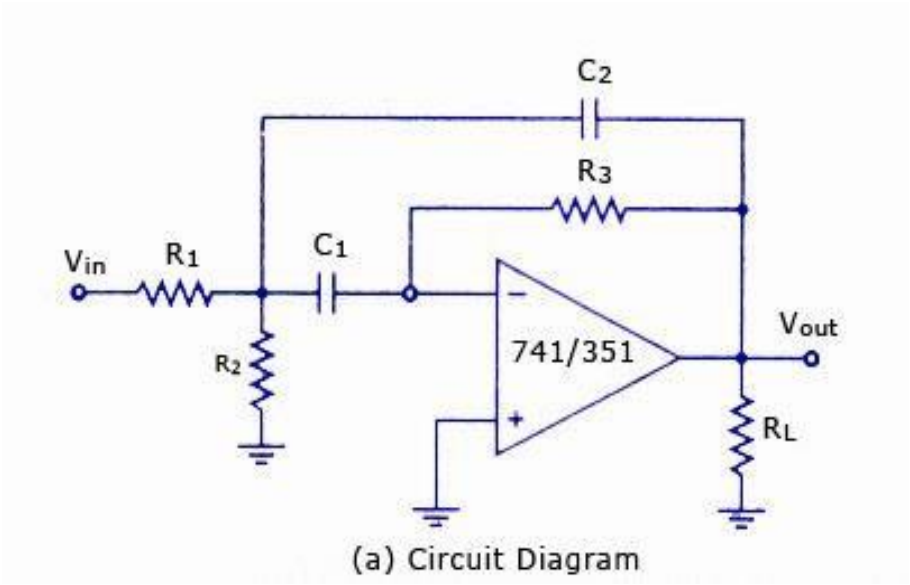
fH=high cut off frequency(Hz)

3.3.2. Narrow Band-Pass Filter

The narrow band-pass filter using multiple feedback is shown in Figure8-13. As shown in this figure, the filter uses only one op-amp. Compared to all the filters discussed so far, this filter is unique in the following respects:

1. It has two feedback paths, hence the name multiple-feedback filter.

2. The op-amp is used in the inverting mode.



(a) Circuit Diagram

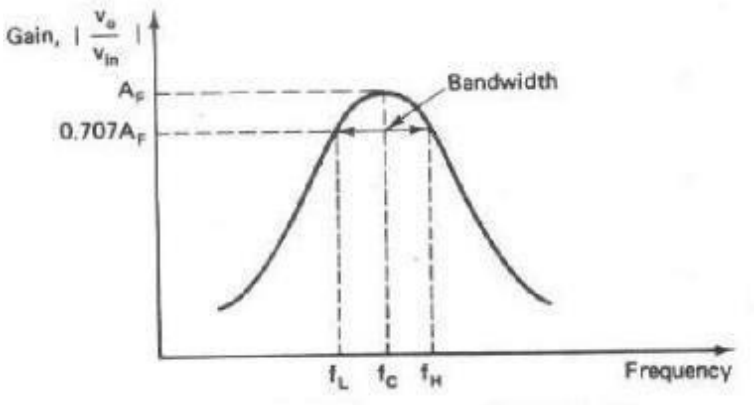


Fig 3.8: (b) Frequency Response

Generally, the narrow band-pass filter is designed for specific values of center frequency *fc* and Q or *fc* and bandwidth. The circuit components are determined from the following relationships. To simplify the design calculations, chooseC1 =C2 =C.

$$R_1 = \frac{Q}{2\pi f_C C A_F}$$ Where AF is the gain at *fc*, given by

$$R_2 = \frac{Q}{\pi f_C C(2Q^2 - A_F)}$$

$$A_F = \frac{R_3}{2R_1}$$

$$R_3 = \frac{Q}{\pi f_C C}$$

The gain *AF*, however, must satisfy the condition

Another advantage of the multiple feedback filter of Figure8-13 is that its center frequency *fc* can be changed to a new frequency ***f'c*** without changing the gain or bandwidth. This is accomplished simply by **changing R2 to R'2 so** that

$$R_2' = R_2\left(\frac{f_C}{f_C'}\right)^2$$

3.4 BAND-REJECT FILTERS

The band-reject filter is also called a band-stop or band-elimination filter. In this filter, frequencies are attenuated in the stop band while they are passed outside this band, as shown in Figure3.1 (d).

As with band-pass filters, the band-reject filters can also be classified as (1)wideband-reject or (2)narrowband-reject. The narrow band-reject filter is commonly called the notch filter. Because of its higher Q (>10), the bandwidth of the narrow band-reject filter is much smaller than that of the wideband- reject filter.

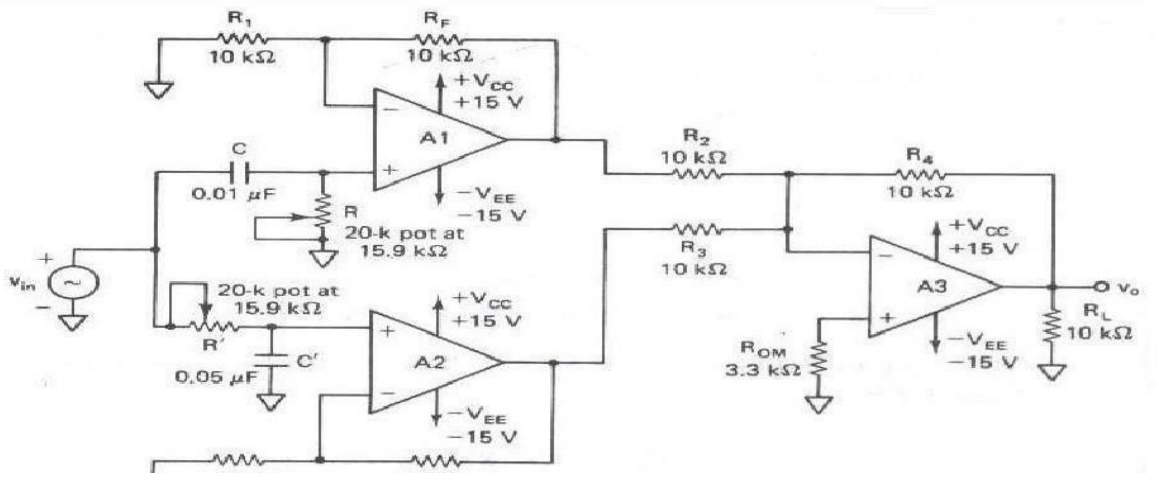


Fig 3.9(a).Wide Band Reject Filter

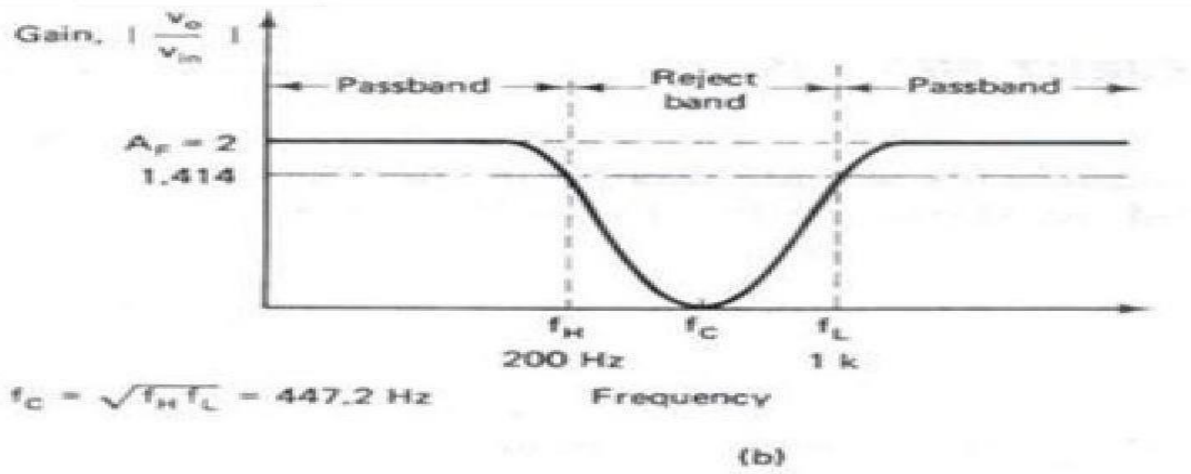


Fig 3.9(b) Frequency Response

Figure 3.9(a) shows a wide band-reject filter using a low-pass filter, a high-pass filter, and assuming amplifier. To realize a band-reject response, the low cut off frequency *fL* of the high- pass filter must be larger than the high cut off frequency *fH* of the low-pass filter. In addition, the pass band gain of both the high-pass and low-pass sections must be equal. The frequency response of the wideband-reject filter is shown in Fig3.9 (b).

3.5 ALL-PASSFILTER

As the name suggests, an all-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different

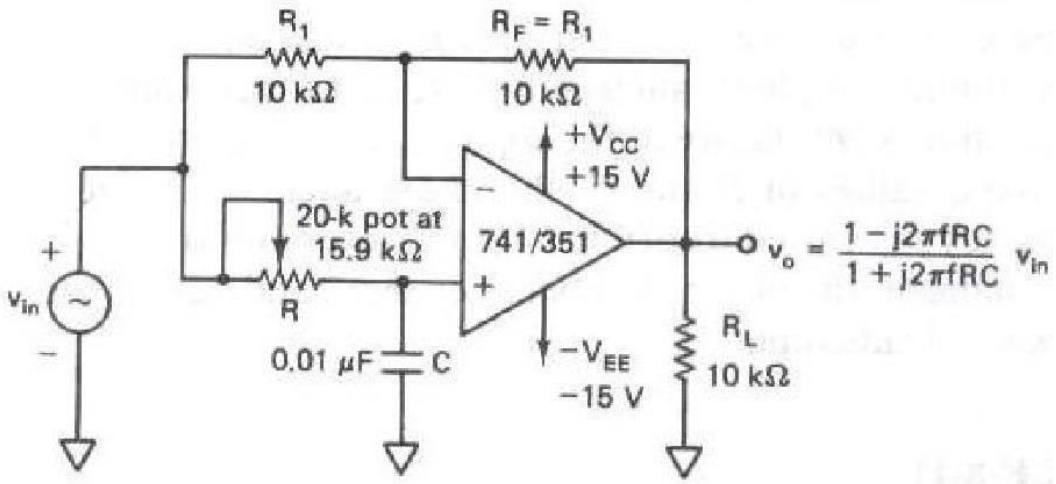


Fig3.11(a)All Pass Filter

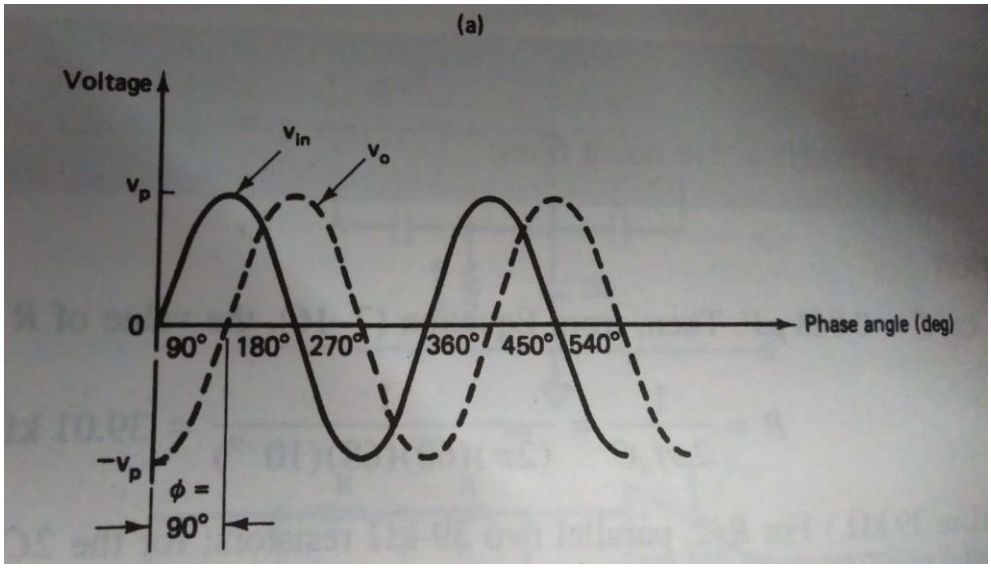


Fig3.11 (b) Phase Shift between Input And Output frequencies of the input signal. When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. To compensate for these phase changes, all-pass filters are required. The all- pass filters are also called delay equalizers or phase correctors.Figure3.11

(a) shows an all-pass filter where in RF =R1. The output voltage Vo of the filter can be obtained by using the superposition theorem:

But **-j =1/j and XC =1/2ΠfC. Therefore, substituting** for XC and simplifying, we get

$$V_o = V_{in}\left(-1 + \frac{2}{j2\pi fRC + 1}\right)$$

$$\frac{V_o}{V_{in}} = \frac{1 - j2\pi fRC}{1 + j2\pi fRC}$$

Where fis the frequency of the input signal in hertz.

Equation indicates that the amplitude of Vo/Vin is unity; that is, |Vo|=|Vin | throughout the useful frequency range, and the phase shift between Vo and Vin is a function of input frequency f. **The phase angle φ** is given by $\phi = -2tan^{-1}\left(\frac{2\pi fRC}{1}\right)$

where **φ** is in degrees, in hertz, R in ohms, and C in farads. Equation is used to find the phase angle **φ** if f, R, and C are known. Figure3 .12 (b) shows a phase shift of 90° between the input Vin and output Vo. That is, Vo lags Vin by90°.For fixed values of R and C, the phase angle **φ** changes from 0 to 180°as the frequency f is varied **from 0 to** ∞**.**InFigure3.12 (a), if the positions of R and C are interchanged, the phase shift between input and output becomes positive. That is, output Vo leads input Vin.

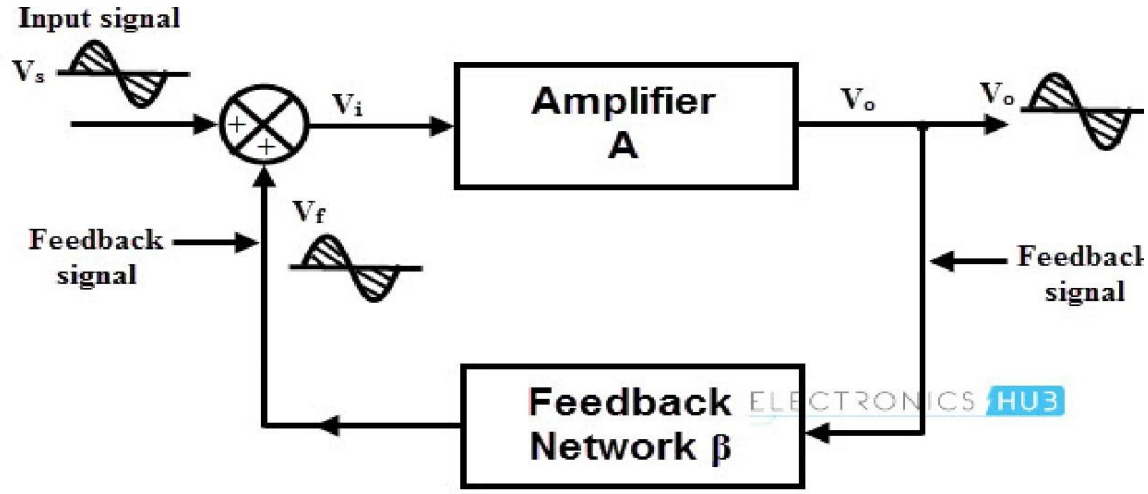
UNIT-IV

3.6 OSCILLATOR TYPES AND PRINCIPLE OF OPERATION

The use of op-amps as oscillators capable of generating a variety of output waveforms. Basically, the function of an oscillator is to generate alternating current or voltage waveforms. More precisely, an oscillator is a circuit that generates are petitive waveform of fixed amplitude and frequency without an y external input signal. Oscillators are used in radio, television, computers, and communications. Although there are different types of oscillators, they all work on the same basic principle.

3.6.1 Oscillator Principle

An oscillator is a type of feedback amplifier in which part of the output is fed back to the input via a feedback circuit. If the signal fed back is of proper magnitude and phase, the circuit produces alternating currents or voltages. To visualize the requirements of an oscillator, consider the block diagram of Figure3.12



However, here the input voltages zero *(Vin*=0). Also, the feedback is positive because most oscillators use positive feedback .Finally; the closed-loop gain of the amplifier is denoted by *Av* rather than *AF*.

Using these relationships, using these relationships, the following equation is obtained:

$$\frac{V_o}{V_{in}} = \frac{A_V}{1 - A_V\beta}$$

However, Vin =0 andVo≠0 implies that *Avβ=1*

Equation gives the two requirements for oscillation:

(1) The magnitude of the loop gain ***AvB*** must be at least1, and
(2) The total phase shift of the loop gain ***AvB*** must be equal to 0°or360°.

If the amplifier uses a phase shift of180°, the feedback circuit must provide an additional phase shift of 180° so that the total phase shift around the loop is 360°.Thewaveforms shown in Figure3.13aresinusoidaland are used to illustrate the circuits action.
The type of waveform generated by an oscillator depends on the components in the circuit and hence maybe sinusoidal, square, or triangular; In addition, the frequency of oscillation is determined by the components in the feedback circuit.

OSCILLATOR TYPES

Types of components used	Frequency of oscillation	Types of waveform generated
RC oscillator *LC* oscillator Crystal oscillator	Audio frequency (AF) Radio frequency (RF)	Sinusoidal Square wave Triangular wave Sawtooth wave, etc.

3.6.2 RC-PHASE SHIFT OSCILLATOR

Figure3.13 shows a phase shift oscillator, which consists of an op-amp as the amplifying stage and three RC cascaded networks as the feedback circuit. The feedback circuit provides feedback voltage from the output back to the input of the amplifier. The op-amp is used in the inverting mode; therefore, any signal that appears at the inverting terminal is shifted by 180° at output.

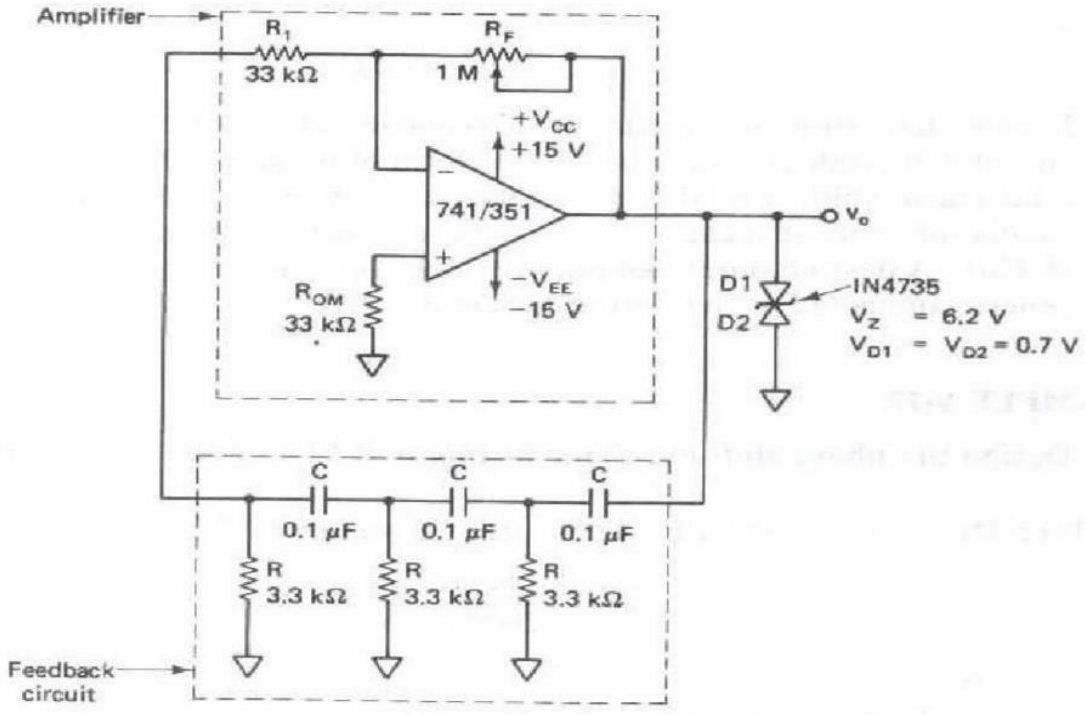


Fig 3.13 RC phase shift Oscillator

An additional 180° phase shift required or oscillation is provided by the cascaded RC networks. Thus the total phase shift around the loop is 360°(or0°). At some specific frequency when the phase shift of the cascaded RC networks is exactly 180°and the gain of the amplifier is sufficiently large, the circuit will oscillate at that frequency. This frequency is called the frequency of oscillation *fo* and is given by

$$f_o = \frac{1}{2\pi\sqrt{6}RC} = \frac{0.065}{RC}$$

At this frequency, the gain *Av* must be at least29.That is,

$$\left|\frac{R_F}{R_1}\right| = 29$$

3.6.3 WIEN BRIDGE OSCILLATOR

Because of its simplicity and stability, one of the most commonly used audio-frequency oscillators is the Wien bridge.Figure3.14 shows the Wien bridge oscillator in which the Wien bridge circuit is connected between the amplifier input terminals and the output terminal. The bridge as a series RC network in one arm and a parallel RC network in the adjoining arm. In the remaining two arms of the bridge, resistorsR1 and RF, are connected. The phase angle criterion for oscillation is that the total phase shift around the circuitmustbe00.Thiscondition occurs only when the bridge is balanced, that is, at resonance. The frequency of oscillation f0 is exactly the resonant frequency of the balanced Wien bridge and is given by

$$f_o = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

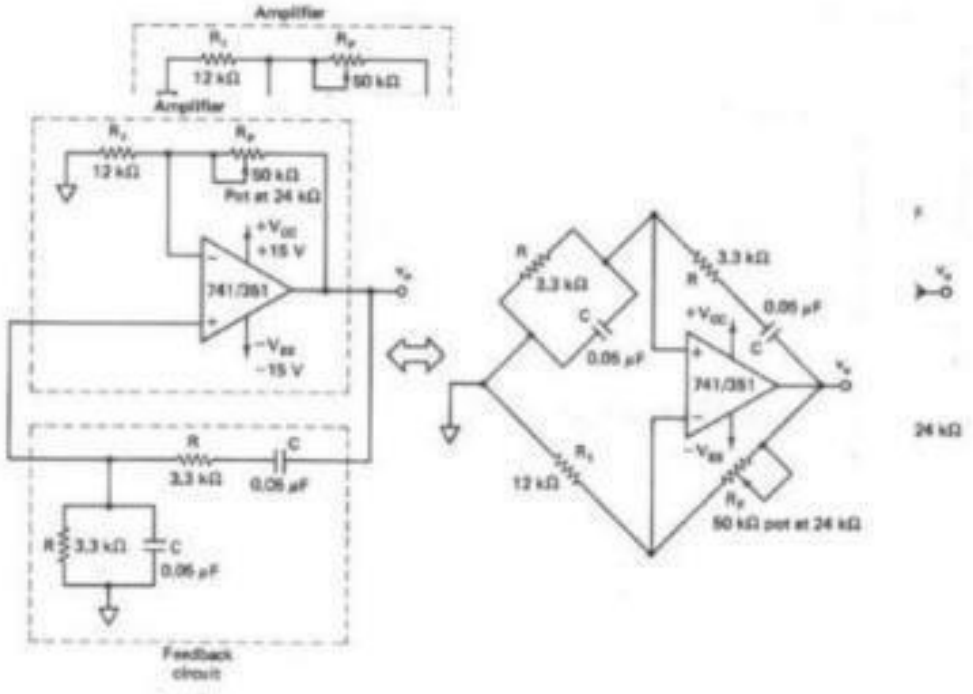


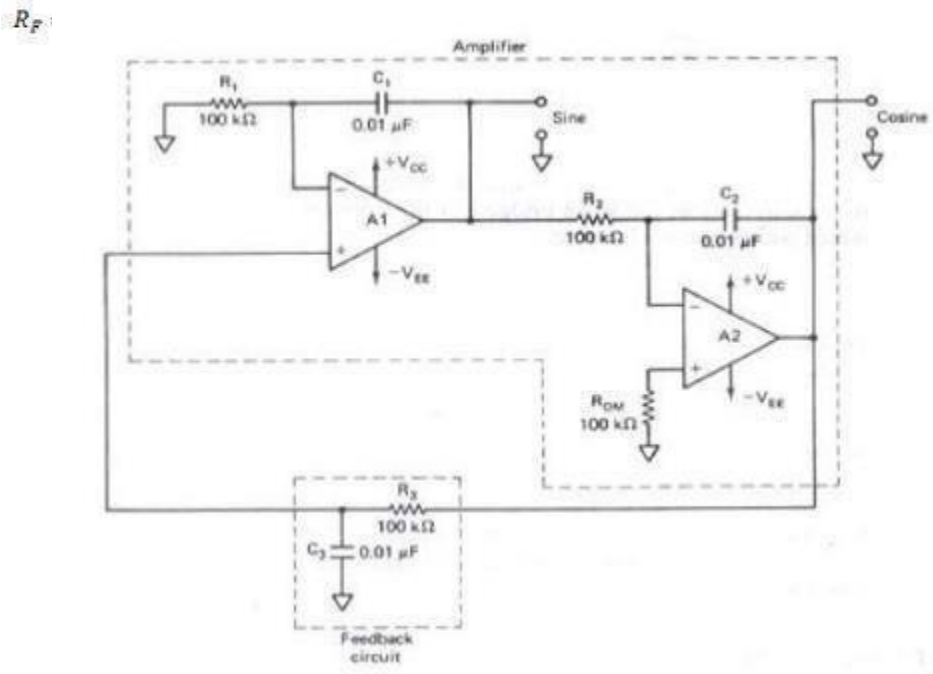
Fig3.14 Wien Bridge

Assuming that the resistors are equal in value, and capacitors are equal in value in the reactive leg of the Wien Bridge. At this frequency the gain required for sustained oscillation is given by

$$A_V = \frac{1}{\beta} = 3$$

$$1 + \frac{R_F}{R_1} = 3$$

3.6.4 QUADRATURE OSCILLATOR



As its name implies, the quadrature oscillator generates two signals (sine and cosine) that are in quadrature, that is, out of phase by 900. Although the actual location of the sine and cosine is arbitrary, in the quadrature oscillator of Figure3.15 the output of A1 is labeled a sine and the output of A2 is a cosine. This oscillator requires a dual op-amp and three RC combinations. The first op-amp A1 is operating in then on-inverting mode and appears as a non-inverting integrator. This condition op-amp A2 is working as a pure integrator.

Furthermore, A2 is followed by a voltage divider consisting of R3 and C3. The divider network forms a feedback circuit, where as A1and A2 form the amplifier stage.

The total phase shift of 360°around the loop required for oscillation is obtained in the following way. The op-amp A2 is a pure integrator and inverter. Hence it contributes-270°or (900) of phase shift. The remaining-90° (or 2700) of phase shift needed are obtained at the voltage divider R3 C3 and the op- amp A1. The total phase shift of 3600, however, is obtained at only one frequency f0,called the frequency of oscillation. This frequency is given by

$$f_o = \frac{1}{2\pi RC}$$

Where R1C1 =R2C2=R3C3=RC. At this frequency,

$$A_V = \frac{1}{\beta} = 1.414$$

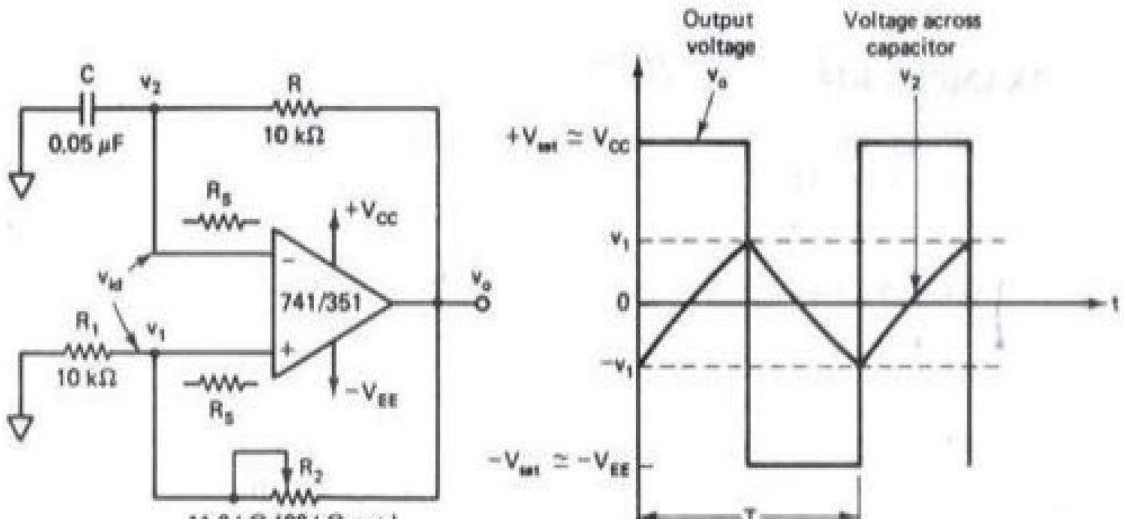
This is the second condition for oscillation. Thus, to design a quadrature oscillator for a desired frequencyf0, choose a value of C; then, from Equation, calculate the value of R. To simplify design calculations, chooseC1 =C2 =C3and R1 =R2 =R3. In addition, R1 may be a potentiometer in order to eliminate any possible distortion in the output waveforms.

3.7 WAVEFORM GENERATORS.

In contrast to sine wave oscillators, square wave outputs are generated when the op-amp is forced to operate in the saturated region. That is, the output of the op-amp is forced to swing repetitively between positive saturation +Vsat **(≈+VCC)** and negative saturation– **Vsat(≈+VEE),** resulting in the square- wave output.

3.7.1 SQUARE WAVE GENERATOR.

One such circuit is shown in Fig3. 16 (a). This square wave generator is also called a **free-running** or **a stable multi vibrator**. The output of the op-amp in this circuit will be in positive or negative saturation, depending on whether the differential voltage **vid** is negative Or positive, respectively.



Assume that the voltage across capacitor C is zero volts at the instant the dc supply voltages +VCC and -VEE are applied. This means that the voltage at the inverting terminal is zero initially. At the same instant, however, the voltage V1 at then on-inverting terminal is a very small finite value that is a function of the output offset voltage VOOT and the values of R1 and R2 resistors. Thus the differential input voltage Vid is equal to the voltage V1 at the non-inverting terminal. Although very small, voltageV1 will start to drive the op-amp into saturation.

For example, suppose that the output offset voltage VOOT is positive and that, therefore, voltage V1 is also positive. Since initially the capacitor C acts as a short circuit, the gain of the op-amp is very large (A); hence V1 drives the output of the op-amp to its positive saturation +Vsat. With the output voltage of the op-amp at +Vsat, the capacitor C starts charging toward +Vsat through resistor R. However, as soon as the voltage V2 across capacitor C is slightly more positive than V1, the output of the op-amp is force dto switch to a negative saturation, -Vsat. With the op-**amp's** output voltage at negative saturation, -Vsat, the voltage v1 across R1 is also negative, since

$$V_1 = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Thus the net differential voltage Vid=V1-V2 is negative, which holds the output of the op-amp in negative saturation. The output remains in negative saturation until the capacitor C discharges and then recharges to a negative voltages lightly higher than-V1. Now, as soon as **the capacitor's voltage** V2 becomes more negative than–V1, the net differential voltage Vid becomes positive and hence drives the output of the op-amp back to its positive saturation +Vsat. This completes one cycle. With output at +Vsat, voltage V1at the non-inverting input is

$$V_1 = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

$$T = 2RC\,ln\left(\frac{2R_1 + R_2}{R_2}\right)$$

The time period T of the output waveform is given by

$$f_o = \frac{1}{2RC\,ln\left(\frac{2R_1 + R_2}{R_2}\right)}$$

Above equation indicates that the frequency of the output f0 is not only a function of the RC time constant but also of the relationship between R1andR2. For example, if R2=1.16R1, Equation becomes

$$f_o = \frac{1}{2RC}$$

3.7.2 TRIANGULARWAVEGENERATOR

Recall that the output waveform of the integrator is triangular if its input is a square wave. This means that a triangular wave generator can be formed by simply connecting an integrator to the square wave generator. The resultant circuit is shown in Figure 3.17(a). This circuit requires a dual op-amp, two capacitors, and at least five resistors.

The frequencies of the square wave and triangular wave are the same. For fixed R1, R2, and C values, the frequency of the square wave as well as the triangular wave depends on the resistance R.

As R is increased or decreased, the frequency of the triangular wave will decrease or increase, respectively. Although the amplitude of the square wave is constant (±Vsat); the amplitude of the triangular wave decreases with an increase in its frequency, and vice versa.

The input of integrator A2 is a square wave, while its output is a triangular wave.

However, for the output of A2 to be a triangular wave requires that 5R3C2>T/2,where T is the period of the square wave input.

R3C2 should be equal toT. To obtain as table triangular wave, it may also be necessary to shunt the capacitor C2 with resistance R4=10R3 and connect an offset voltage-compensating network at the non-inverting terminal of A2.

Another triangular wave generator, which requires fewer components is shown in Fig 3. 1 8 (a). The generator consists of a comparator A1, and an integrator A2. The comparator A1 compares the voltage at point P continuously with the inverting input that is at 0V.When the voltage at P goes slightly below or above 0V, the output of A1 is at the negative or positive saturation level, respectively.

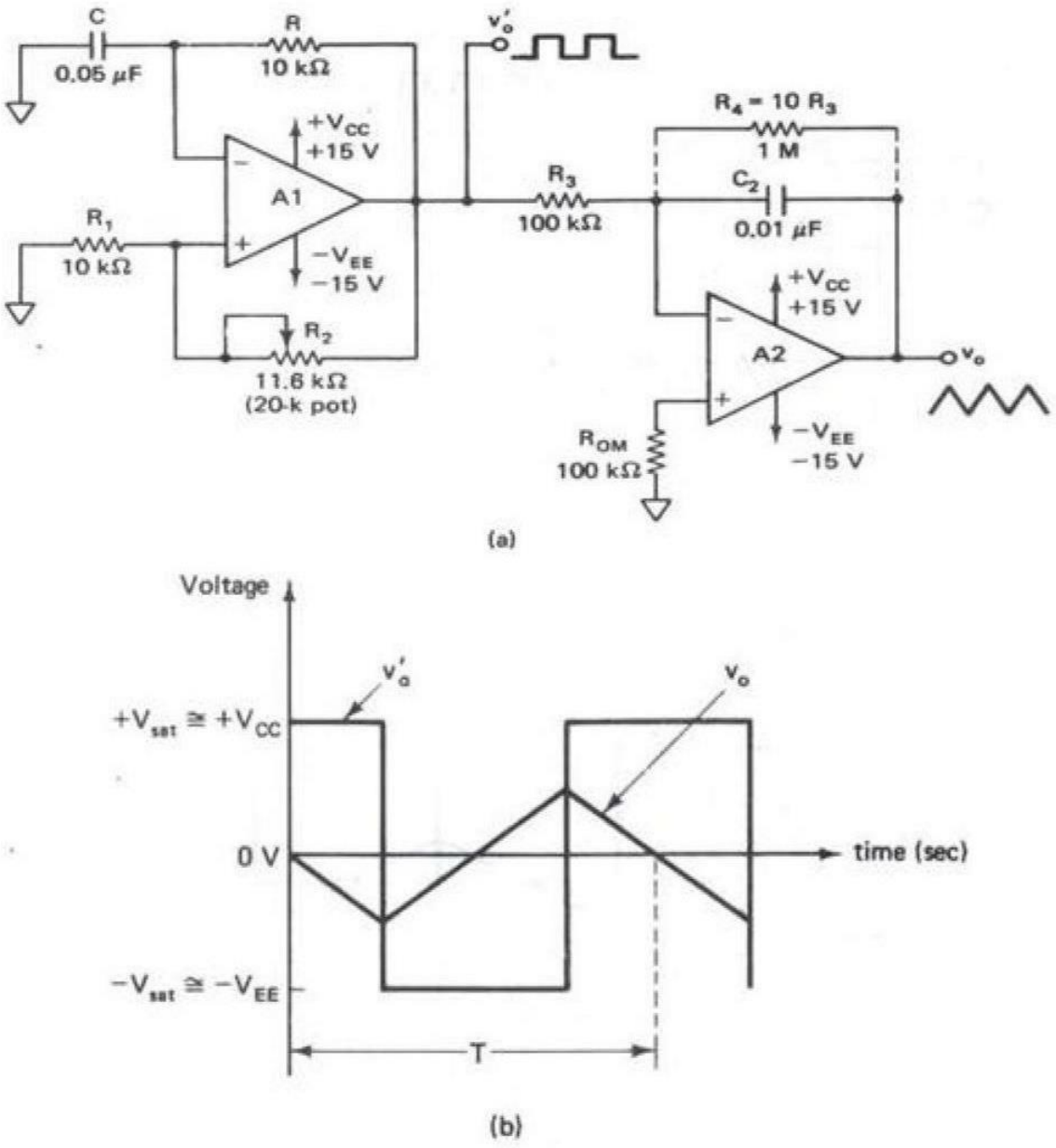


Fig.3.17: (a) Triangular Wave Generator (b) Output Wave Form

To illustrate the **circuit's** operation, let us set the output of A, at positive saturation +V(+Vc). This +V is an input of the integrator A2. The output of A2, therefore it will be a negative-going ramp. Thus one end of the voltage-divider R2-R3 is the positive saturation voltage +V of A, and the other is the negative-going ramp of A2. When the negative-going ramp attains a certain value V Ramp, point P is slightly below 0 V; hence the output of A1 will switch from positive saturation to negative saturation. This means that the output of A2 will now stop going negatively and will begin to go positively. The output of A2 will continue to increase until it reaches +At this time the point P is slightly above 0V; therefore, the output of A, is switched back to the positive saturation level +V. The sequence then repeats. The output waveform is as shown in Figure3.18(b).

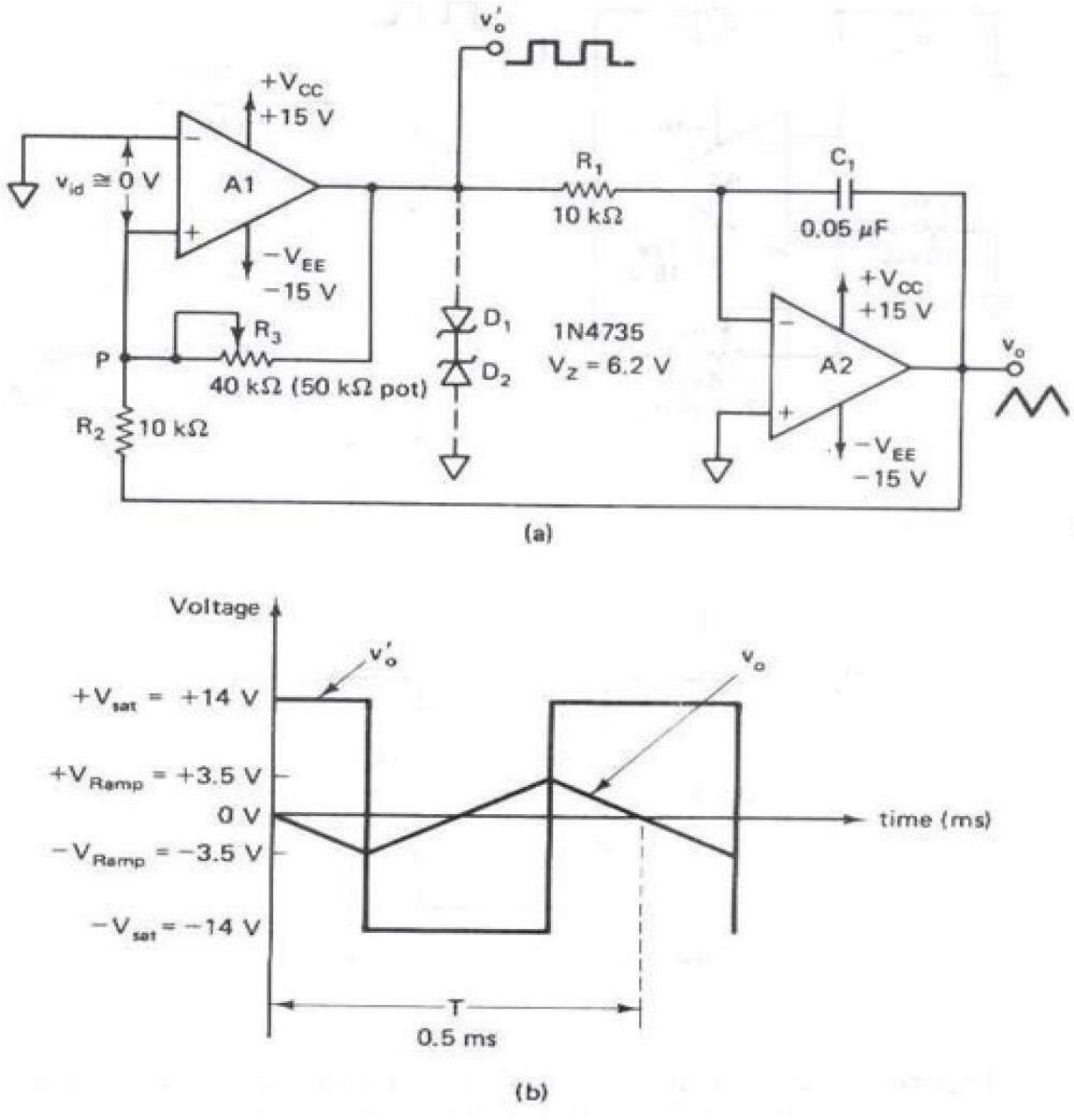


Fig 3.18 Triangular Wave Generator (a)Circuit (b)Input and Output Waveform

The frequencies of the square wave and the triangular wave are the same. The amplitude of the square wave is a function of the dc supply voltages. However, a desired amplitude can be obtained by using appropriate zeners at the output of A1.

The amplitude and the frequency of the triangular wave can be determined as follows: From Figure3.18(b),when the output of the comparator A1 is +V, the output of the integrator A2 steadily decreases until it reaches—Vrn,.At this time the output of A1 switches from +V to -V. Just before this switching occurs, the voltage at point P (+input) is 0V. This means that the —V Ramp must be developed across R2, and +Vsat must be developed across R3. That is,

$$\frac{-V_{Ramp}}{R_2} = -\frac{+V_{sat}}{R_3}$$

$$-V_{Ramp} = -\frac{R_2}{R_3}(+V_{sat})$$

Similarly, +Vj,, the output voltage of A2 at which the output of A1 switches from –V to +V, is given by.

$$+V_{Ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

The peak-to-peak (pp) output amplitude of the triangular wave is

$$V_o(pp) = +V_{Ramp} - (-V_{Ramp})$$

$$V_o(pp) = 2\frac{R_2}{R_3}(V_{sat})$$

Above equation indicates that the amplitude of the triangular wave decreases with an increase in R3.

The time it takes for the output waveform to swing from— to + (or from +V Ramp to — V Ramp) is equal to half the time period T/2.This time can be calculated from the integrator output equation.

$$V_o(pp) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

The frequency of oscillation then is

$$f_o = \frac{R_3}{4R_1C_1R_2}$$

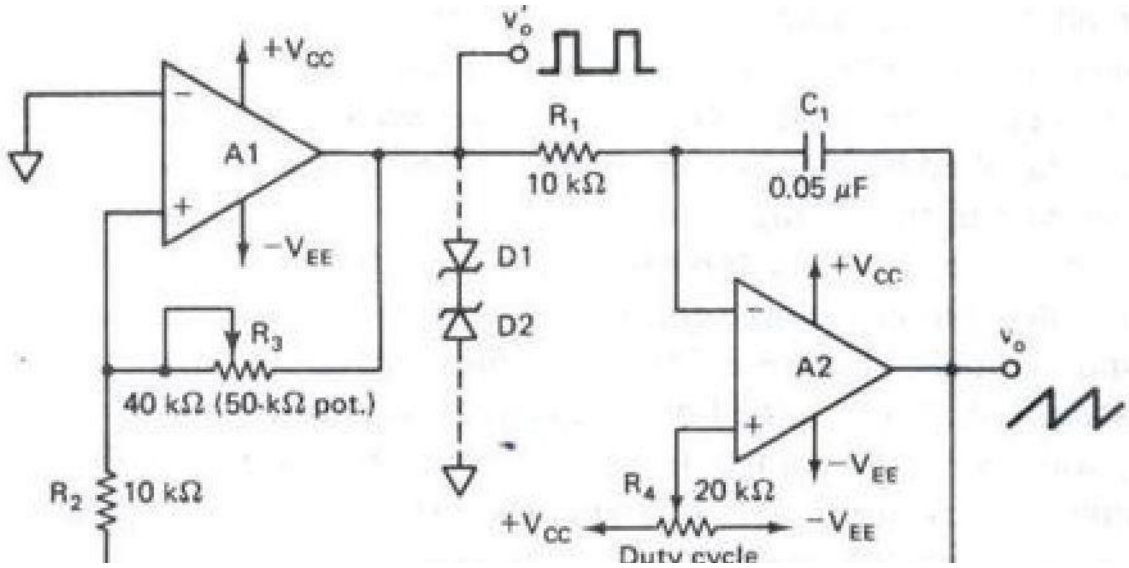
3.7.3 SAWTOOTH WAVEGENERATOR

The difference between the triangular and sawtooth waveforms is that the rise-time of the triangular wave is always equal to its fall-time. That is, the same amount of time is required for the triangular wave to swing from –Vramp to +Vramp as from +Vramp to-Vramp. On the other hand, the sawtooth waveform has unequal rise and fall times. That is, it may rise positively many times faster than it falls negatively, or vice-versa.

The triangular wave generator of Figure3.19(a) can be converted into a sawtooth wave generator by injecting a variable dc voltage into the non-inverting terminal of the integrator A2. This can be accomplished by using the potentiometer and connecting it to the +VCC and-VEE as shown in Figure 3.19(a).

Depending on the R4 setting, a certain dc level is inserted in the output of A2. Now, suppose that the output of A1 is a square wave and the potentiometer R4 is adjusted for a certain dc level.

This means that the output of A2 will be a triangular wave, riding on some dc level that is a function of the R4 setting. The duty cycle of the square wave will be determined by the polarity and amplitude of this dc level. A duty cycle less than 50% will then cause the output of A2 to be a sawtooth.



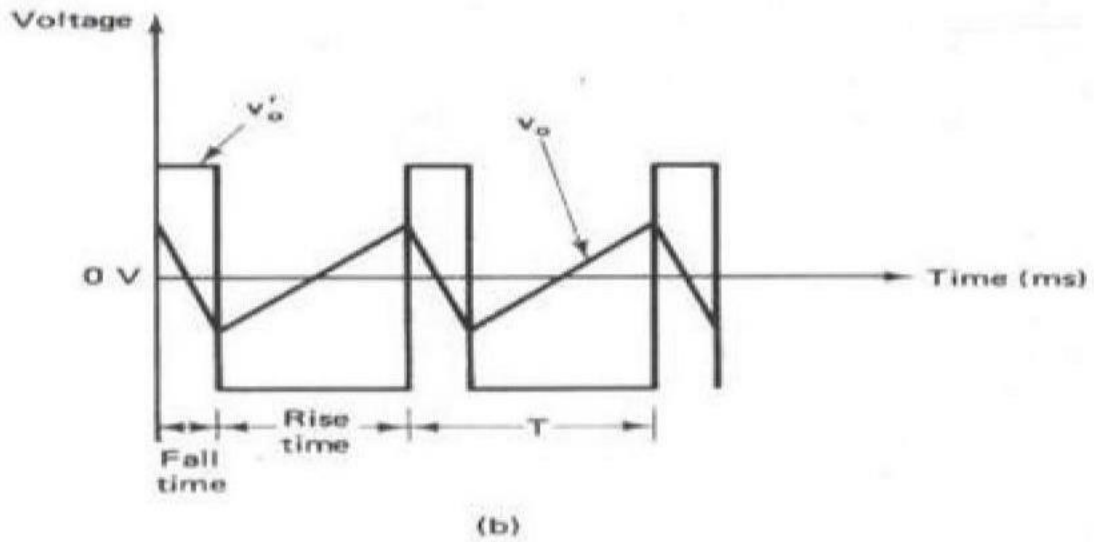


Fig 3.19 Sawtooth Wave generator (a) Circuit (b)Output Waveform With the wiper at the center of R4, the output of A2 is a triangular wave.

For any other position of R4 wiper, the output is a sawtooth waveform. Specifically as the R4 wiper is moved toward— V, the rise-time of the sawtooth wave becomes longer than the fall time. On the other hand, as the wiper is moved toward +Vcc, the fall time becomes longer than the rise-time. Also, the frequency of the sawtooth wave decreases as R4is adjusted toward + V or — VEE. However, the amplitude of the sawtooth wave is independent of theR4setting.

3.8 VOLTAGE CONTROLLED OSCILLATOR:

In all the preceding oscillators the frequency is determined by the RC time constant. However there are applications, such as frequency modulation, tone generators and frequency keying, where the frequency needs to be controlled by means of an input voltage called controlled voltage. This function is achieved in the voltage controlled oscillator (VCO) also called a voltage to frequency converter. A typical example is the signetics NERSE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. Figure(b) is a block diagram of 566,the frequency of oscillation is determined by an external resistor R1 and capacitor C1 and the voltage Vc applied to the control terminal 5.The triangular wave is generated by alternately charging the external capacitor C1 by one current source and then linearly discharging it by another. The discharge levels are determined by schmitt trigger action. The schmitt trigger also provides the square wave output. Both the output wave forms are buffered so that the output impedance of each is 50ohms.The typical amplitude of the triangular wave is 2.4 volts peak to peak and that of the square wave is 5.4 volts peak to peak.

TIMERS

2.1 INTRODUCTION TO 555 TIMER:

One of the most versatile linear integrated circuits is the *555* timer. A sample of these applications includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. The timer basically operates in one of the two modes: either as monostable (one-shot) multivibrator or as an astable (free running) multivibrator. The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP.

The SE555 is designed for the operating temperature range from - 55°Cto + 125°C, while the NE555 operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it operates on +5 to + 18 V supply voltage in both free-running (astable) and one- shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds through hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C.

Like general-purpose op-amps, the 555 timer is reliable, easy to us, and low cost.

Pin 1: Ground.
All voltages are measured with respect to this terminal.

Pin 2: Trigger.

The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 VCC. However, when a negative-going pulse of amplitude larger than 1/3 VCC is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin 3: Output.

There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage + VCC (pin 8). When the output is low,

the load current flows through the load connected between pin 3 and + VCC into the output terminal and is called the sink current.

However, the current through the grounded load is zero when the output is low. For this reason, the load connected between pin 3 and + VCC is called the normally on load and that connected between pin 3 and ground is called the normally off load.

On the other hand, when the output is high, the current through the load connected between pin 3and + VCC (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the source current. The maximum value of sink or source current is 200 mA.

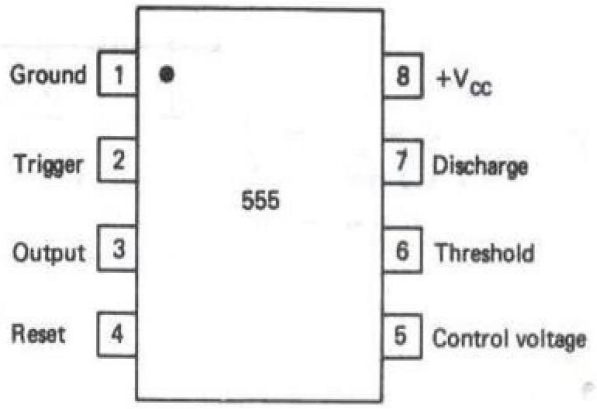


Fig 2.1: Pin diagram of 555Timer

Pin 4: Reset.

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + VCC to avoid any possibility of false triggering.

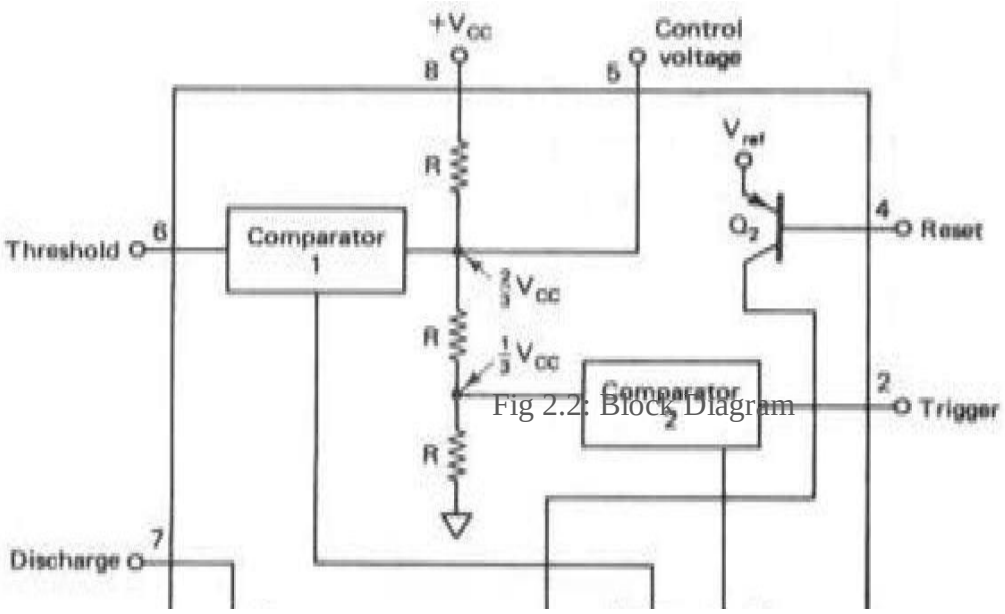


Fig 2.2: Block Diagram

Pin 5: Control voltage.

An external voltage applied to this terminal changes the threshold as well as the trigger voltage . In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01-**µF capacitor to prevent any** noise problems.

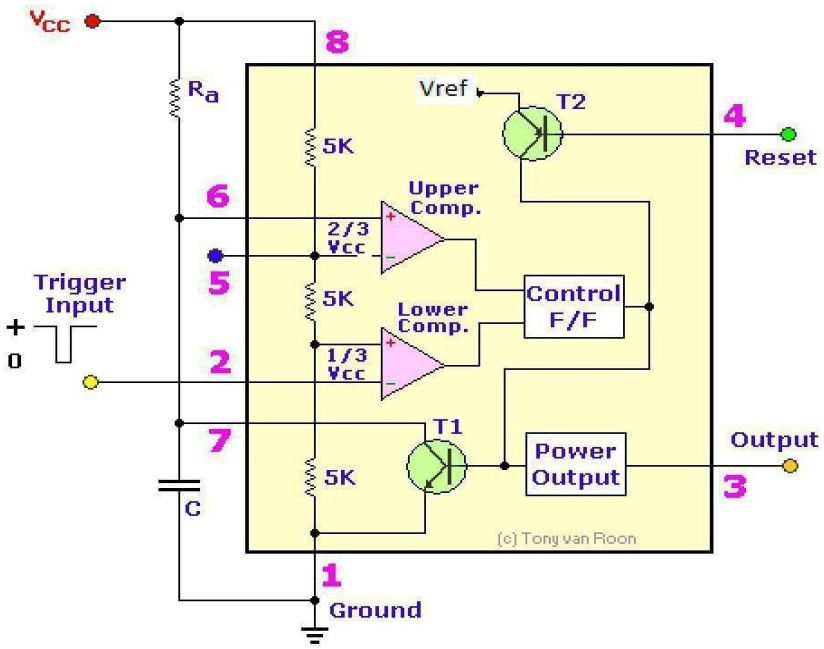
Pin 6: Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage across the external capacitor. When the voltage at this pin is threshold voltage 2/3 V, the output of comparator 1 goes high, which in turn switches the output of the timer low.

Pin 7: Discharge. This pin is connected internally to the collector of transistor Q1, as shown in Figure 2.1(b). When the output is high, Q1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin 8: + VCC.

The supply voltage of +5 V to +18 is applied to this pin with respect to ground (pin1).

2.2 FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER:



Block diagram of timer

2.3 THE 555 AS A MONOSTABLE MULTIVIBRATOR

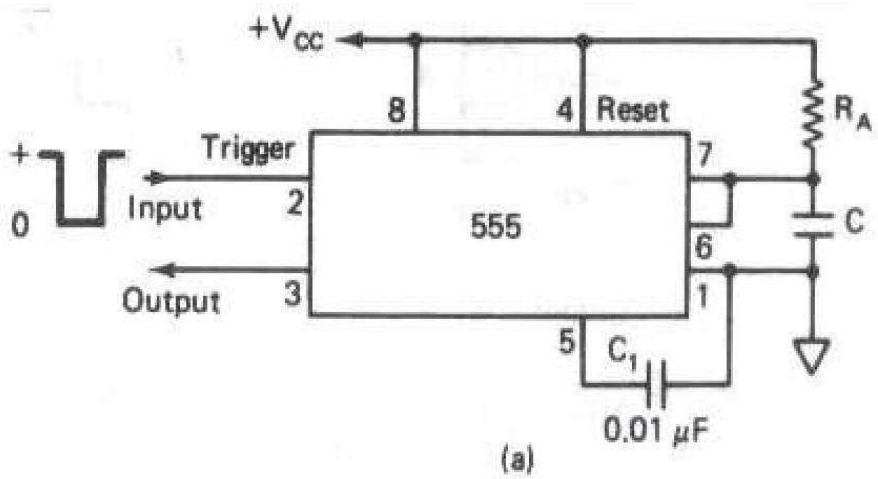
A monostable multivibrator, often called a one-shot multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the circuit is approximately zero or at logic-

\low level. When an external trigger pulse is applied, the output is forced to go high (≈VCC).

The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats.

The monostable circuit has only one stable state (output low), hence the name mono-stable. Normally, the output of the mono- stable multivibrator is low. Fig 2.2 (a) shows the **555 configured for monostable operation. To better explain the circuit's operation, the** internal block diagram is included in Fig 2.2(b).



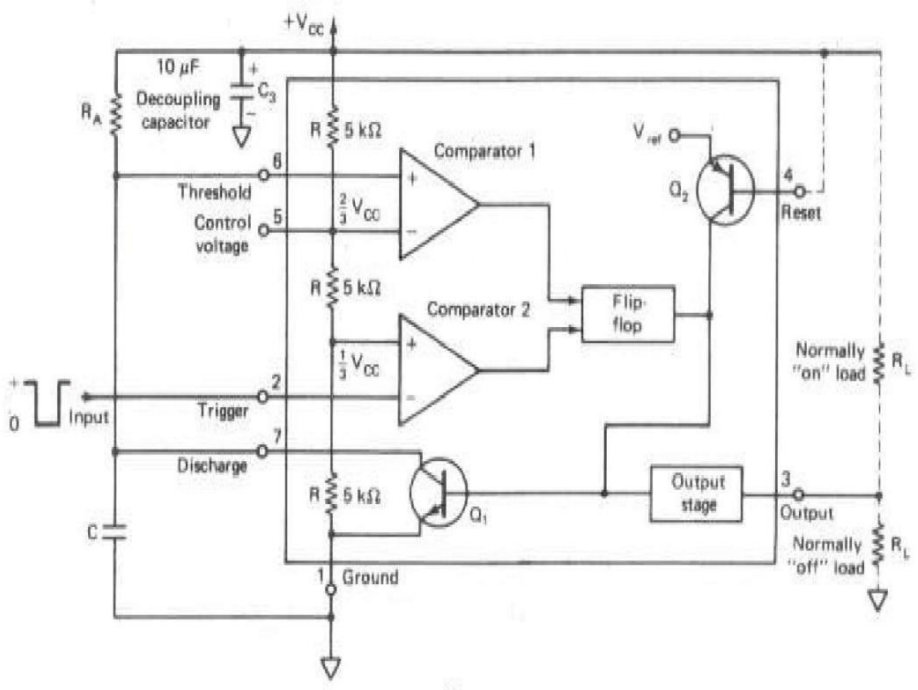
(a)

Mono-stable operation:

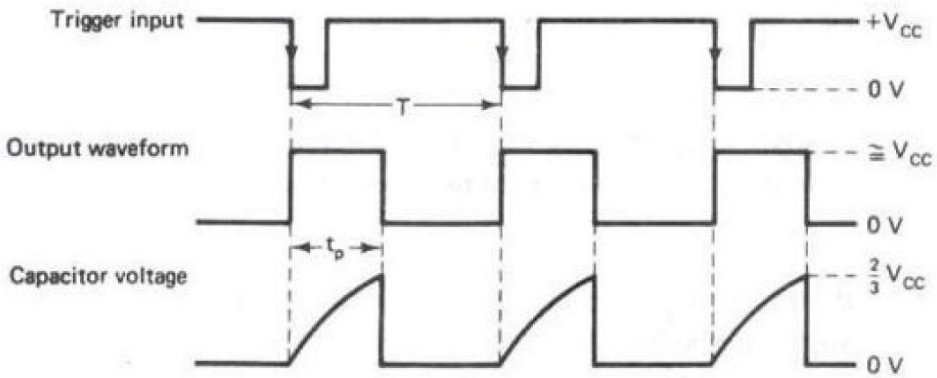
According to Fig 2.2(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward Vcc through RA.

However, when the voltage across the capacitor equals 2/3 Va., comparator **I 's output** switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q on, and hence capacitor C rapidly discharges through the transistor.

The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 4-2(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 the time during which the output remains high is given by where Fig.2.5 (b) 555 connected as a Monostable Multivibrator (c) input and output waveforms Where RA is in ohms and C is in farads. Figure 2.2(c) shows a graph of the various combinations of RA and C necessary to produce desired time delay



(b)



(c)

Note that this graph can only be used as a guideline and gives only the approximate value of RA and C for a given **time delay. Once triggered, the circuit's output will remain in the high state until the set time**1, elapses. The output will not change its state even if an input trigger is applied again during this time interval T. However, the circuit can be reset during the timing cycle by applying a negative pulse to the reset terminal. The output will then remain in the low state until a trigger is again applied.

Often in practice a decoupling capacitor (10 F) is used between +(pin 8) and ground (pin 1) to eliminate unwanted voltage spikes in the output waveform. Sometimes, to prevent any possibility of mistriggering the monostable multivibrator on positive pulse edges, a wave shapingcircuit consisting of R, C2, and diode D is connected between the trigger input pin 2 and pin 8, as shown in Figure 4-3. The values of R and C2 should be selected so that the time constant RC2 is smaller than the output pulse width.

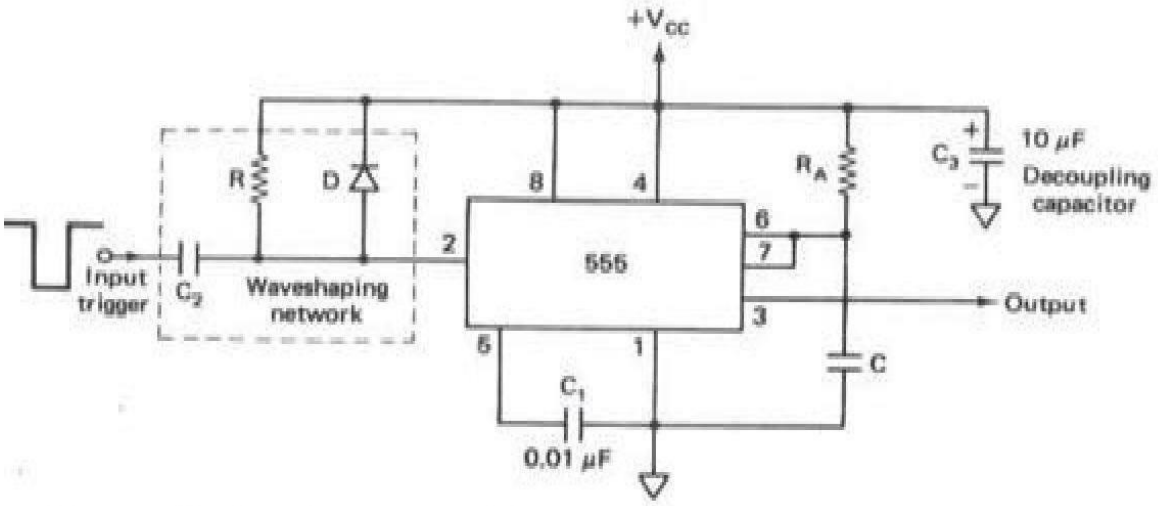


Fig.2.6: Monostable Multivibrator with wave shaping network to prevent +ve pulse edge triggering

Monostable Multivibrator Applications

Frequency divider: The monostable multivibrator of Figure 2.2(a) can be used as a frequency divider by adjusting the length of the timing cycle tp, with respect to the tine period T of the trigger input signal applied to pin 2. To use monostable multivibrator as a divide-by-2 circuit, the timing interval tp must be slightly larger than the time period T of the trigger input signal, as shown in Figure 2.4. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, tp must be slightly larger than twice the period of the input trigger signal, and so on. The frequency-divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.

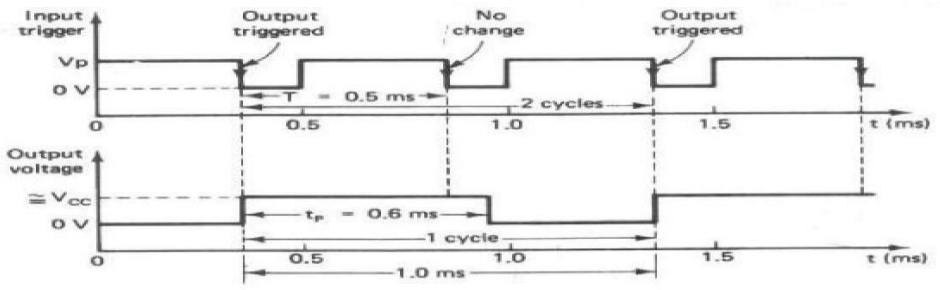


Fig 2.7 input and output waveforms of a monostable multi vibrator as a divide-by-2 network

(b) **Pulse stretcher:** This application makes use of the fact that the output pulse width (timing interval) of the rnonostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name pulse stretcher. Often, narrow-pulse- width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time. The 555 pulse stretcher can be used to remedy this problem

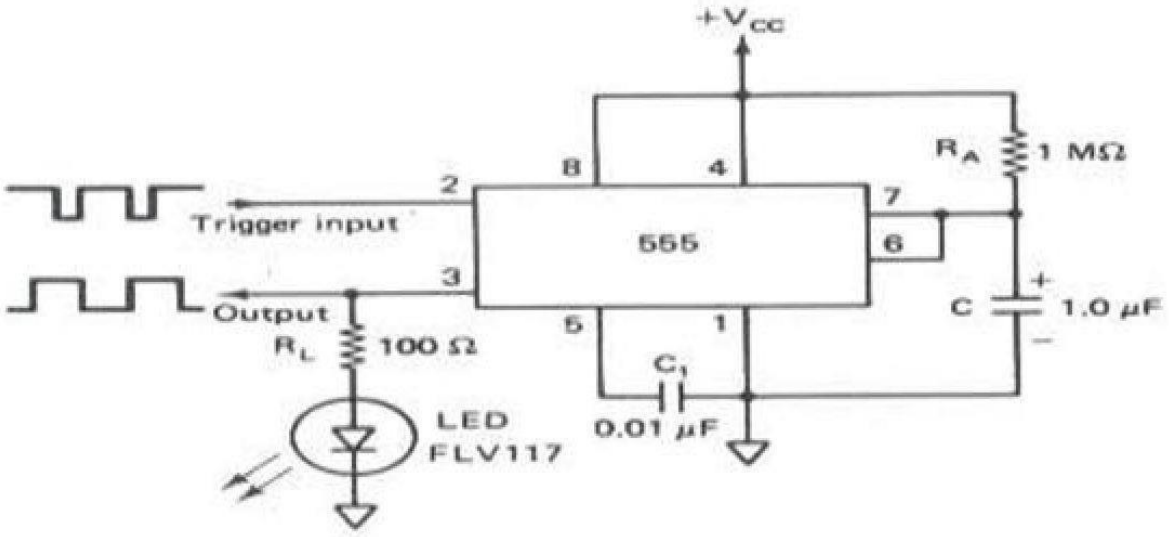
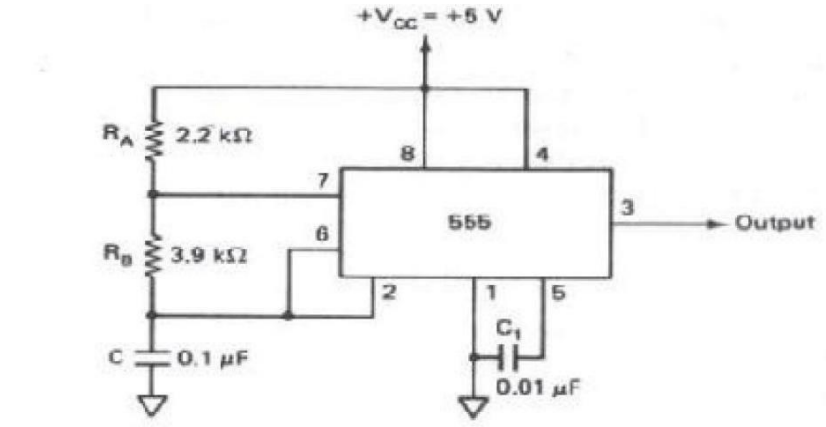


Fig 2.8 Monostable multi vibrator as a Pulse stretcher

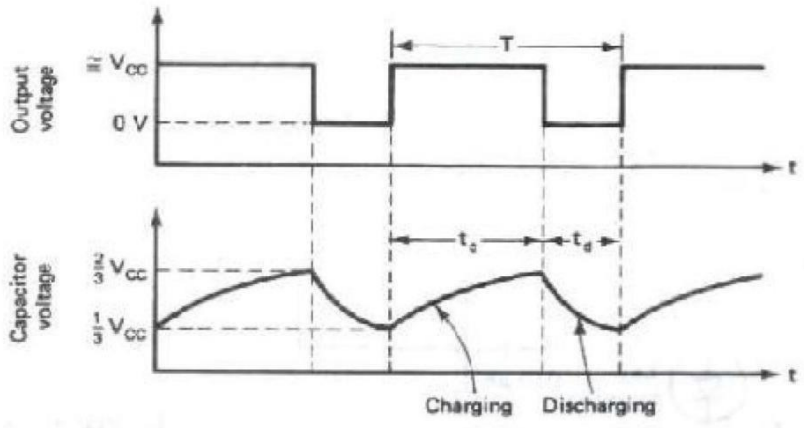
Figure 2.8 shows a basic monostable used as a pulse stretcher with an LED indicator at the output. The LED will be on during the timing interval tp = 1.1RAC, which can be varied by changing the value of RA and/or C.

2.4 THE 555 AS AN ASTABLE MULTIVIBRATOR:

The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular- wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig 4-6(a) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and R8. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low. Now capacitor C starts discharging through R8 and transistor Q. When the voltage across C **equals 1/3 comparator 2's output triggers the flip**-flop, and the output goes high. Then the cycle repeats.



(a)



(b)

Fig 2.9: The 555 as a Astable Multivibrator (a)Circuit(b)Voltage across Capacitor and O/P waveforms.

The output voltage and capacitor voltage waveforms are shown in Figure 2.6(b). As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 V, respectively. The time during which the capacitor charges from 1/3 V to 2/3 V. is equal to the time the output is high and is given by

$$t_C = 0.69(R_A + R_B)C$$

where RA and R3 are in ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 V to 1/3 V is equal to the time the output is low and is given by

$$t_d = 0.69(R_B)C$$

where RB is in ohms and C is in farads. Thus the total period of the output waveform is

$$T = t_C + t_d = 0.69(R_A + 2R_B)C$$

This, in turn, gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Above equation indicates that the frequency fo is independent of the supply voltage V. Often the term duty cycle is used in conjunction with the astable multivibrator . The duty cycle is the ratio of the time t during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,

$$\%\, duty\, cycle = \frac{t_C}{T} \times 100$$

$$= \frac{R_A + 2R_B}{R_A + 2R_B} \times 100$$

Astable Multivibrator Applications:

Square-wave oscillator: Without reducing RA = 0 , the astable multivibrator can be used to produce a square wave output simply by connecting diode D across resistor RB, as shown inFigure 4-7. The capacitor C charges through RA and diode D to approximately 2/3 Vcc anddischarges through RB and terminal 7 until the capacitor voltage equals approximately 1/3 Vcc; then the cycle repeats. To obtain a square wave output (50% duty cycle), RA must be a
combination of a fixed resistor and potentiometer so that the potentiorneter can be adjusted for exact square wave.

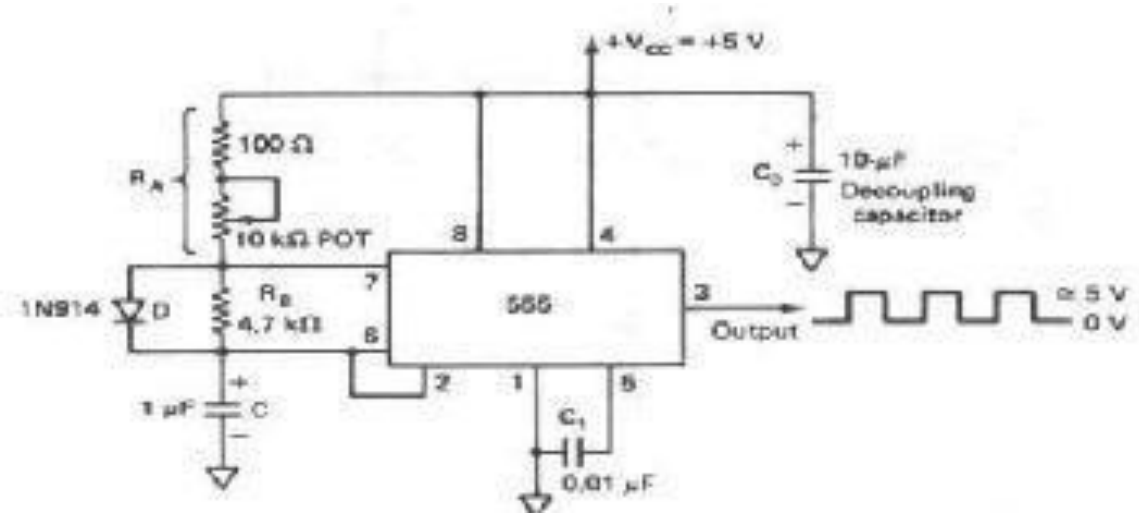


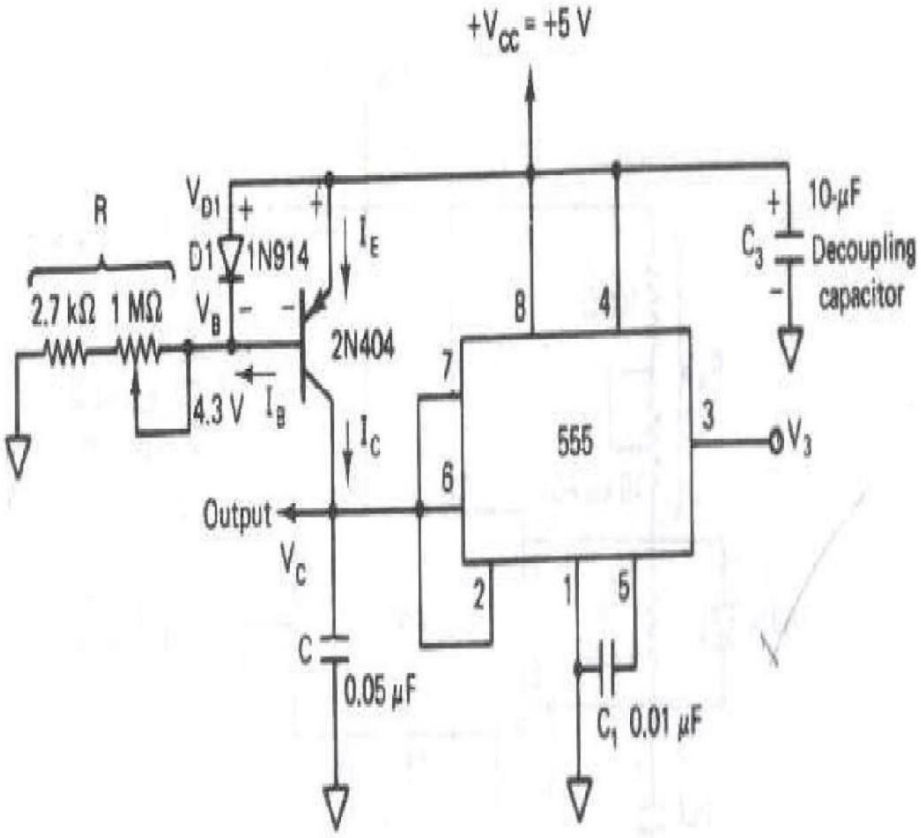
Fig 2.10: Astable Multivibrator as a Square wave generator **Free-running ramp generator:** The astable multivibrator can be used as a free-running ramp generator when resistors RA and R3 are replaced by a current mirror. Figure 2.8(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward Vcc at a constant rate.
When voltage across C equals 2/3 Vcc, comparator 1 turns transistor Q on, and C rapidly discharges through transistor Q. However, when the discharge voltage across C is

approximately equal to 1/3 Vcc, comparator 2 switches transistor Q off, and then capacitor C starts charging up again. Thus the charge— discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time and is approximately given by

$$T = \frac{V_{cc}C}{3I_C}$$

Where I = (Vcc — VBE)/R = constant current in amperes and C is in farads. Therefore, the free running frequency of the ramp generator is

$$f_o = \frac{3I_C}{V_{cc}C}$$



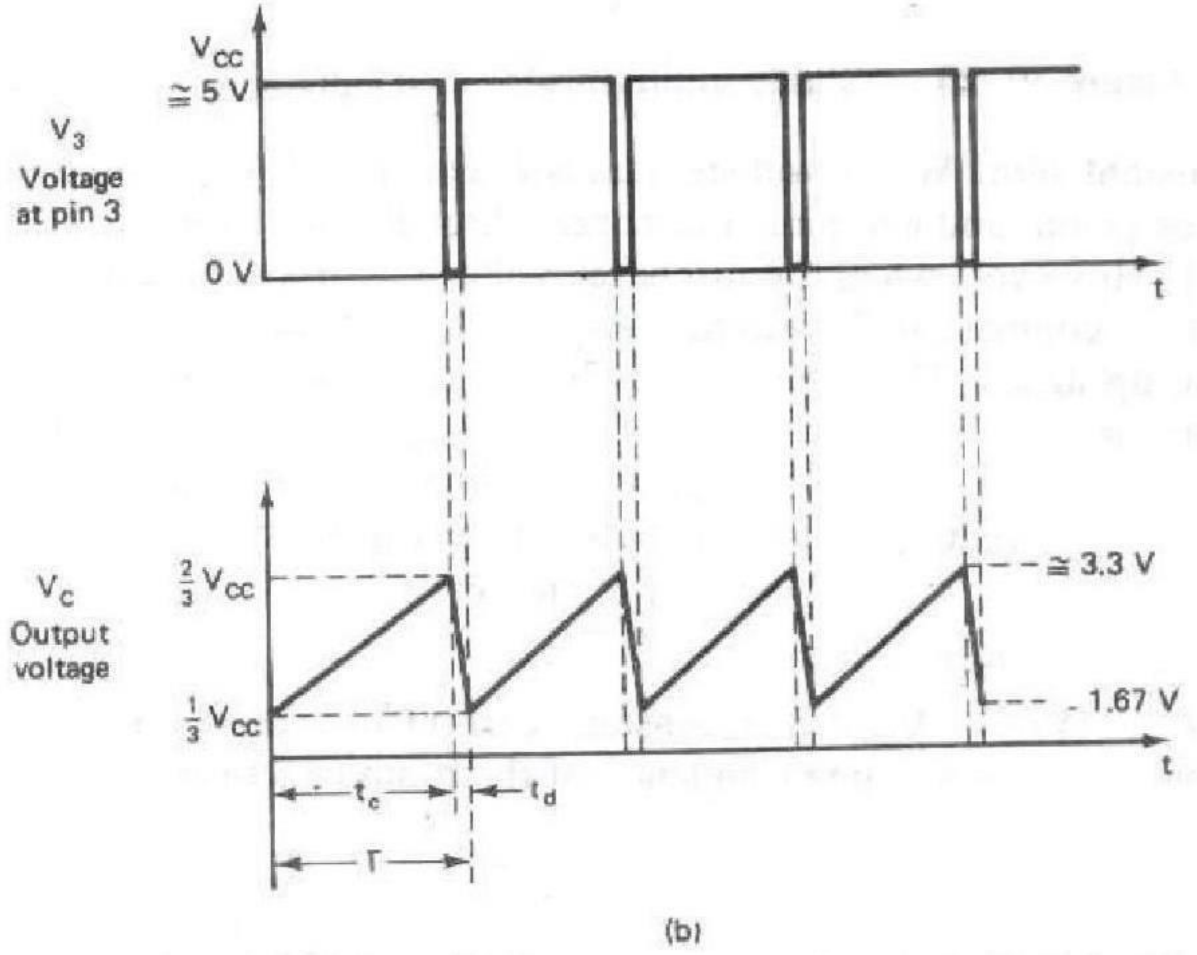


Fig 2.11: (a) Free Running ramp generator (b) Output waveform.

2.5 SCHMITT TRIGGER:

The below fig 2.9 shows the use of 555 timer as a Schmitt trigger:

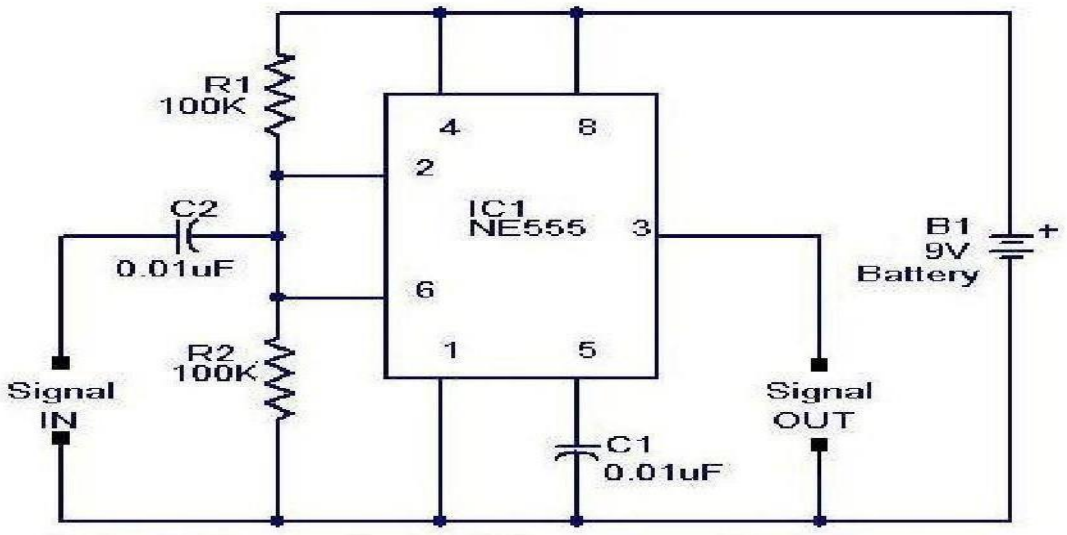


Fig 2.12: Timer as Schmitt trigger

the input is given to the pin 2 and pin 6 which are tied together. Pins 4 and 8 are connected to supply voltage +Vcc. The common point of two pins 2 and 6 are externally biased at Vcc/2 through the resistance network R1 and R2.Generally R1=R2 to the gate biasing of Vcc/2.The upper comparator will trip at 2/3Vccwhile lower comparator at 1/3Vcc.The bias provided by R1 and R2 is centered within these two thresholds. Thus when sine wave of sufficient amplitude, greater than Vcc/6 is applied to the circuit as input, it causes the internal flip flop to alternately set and reset. Due to this, the circuit produces the square wave at the output.

2.6 PHASE-LOCKED LOOPS

The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in TV and in FM tuners.

Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase-locked loop.

2.6.1 Bloch Schematic and Operating Principle

Figure 2.10 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure, the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and, (3) a voltage controlled oscillator

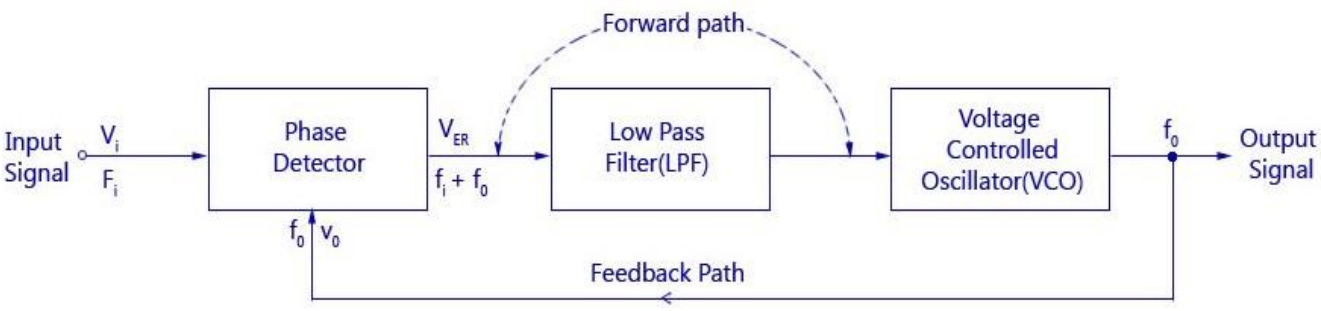


Fig 2.13: Block Diagram of Phase Locked Loop

The phase detectors or comparator compares the input frequency *f*IN with the feedback frequency *f*OUT.. The output voltage of the phase detector is a dc voltage and therefore is

often referred to as the error voltage. The output of the phase is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level.

This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: free- running, capture, and phase lock. Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase- locked loop is then in the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action. Before studying the specialized phase-locked-loop IC, we shall consider the discrete phase-locked loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled oscillator.

(a) Phase detector:

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity.

A double-balanced mixer is a classic example of an analog phase detector. On the other hand,examples of digital phase detectors are these:

1. Exclusive-OR phase detector

2. Edge-triggered phase detector

3. Monolithic phase detector (such as type 4044)

The following fig 2.11 shows Exclusive-OR phase detector:

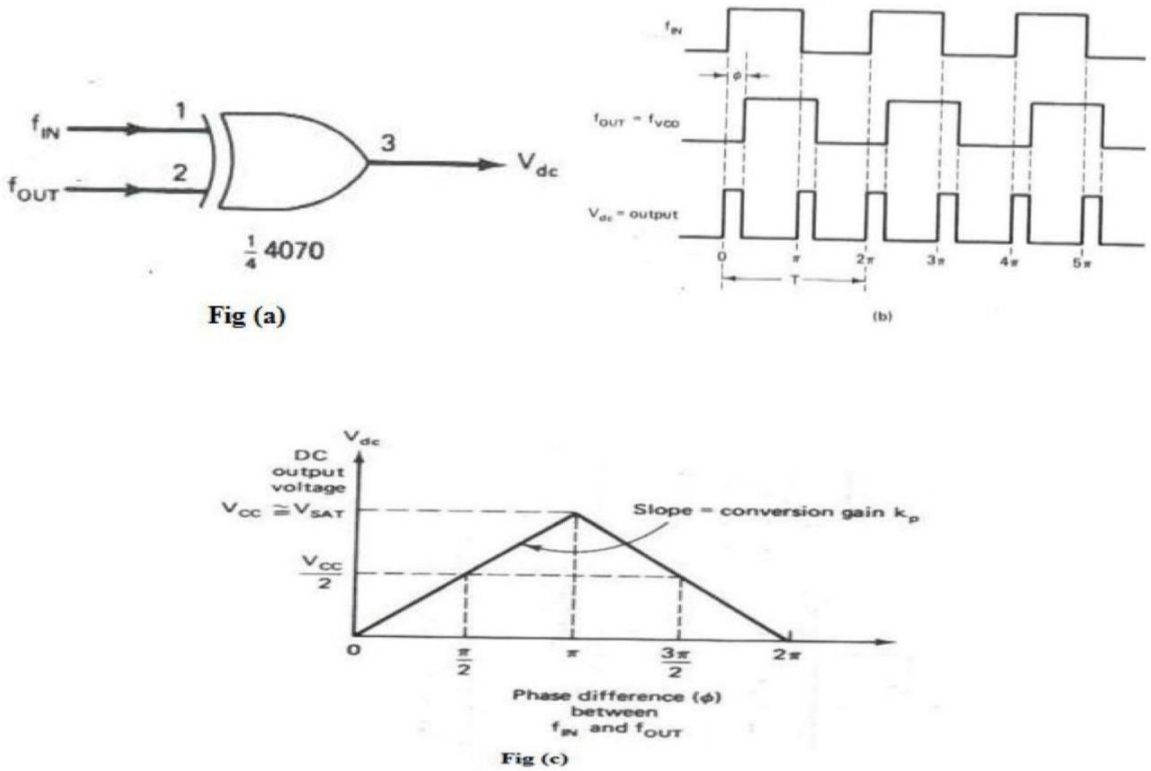


Fig 2.14 (a) Exclusive-OR phase detector: connection and logic diagram. (b) Input and output waveforms. (c) Average output voltage versus phase difference between *f*IN and *f*OUT curve.

(b) Low-pass filter

The function of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

More important, the 1ow-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency *f*IN. An equivalent term for lock range is tracking range. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

(c) Voltage-controlled oscillator:

A third section of the PLL is the voltage-controlled oscillator. The VCO generates an output frequency that is directly proportional to its input voltage. Typical example of VCO is Signetics NE/SE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. The block diagram of the VCO is shown in Fig 2.12. The frequency of oscillations is determined by three external R1 and capacitor C1 and the voltage VC applied to the control terminal 5

The triangular wave is generated by alternatively charging the external capacitor C1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms.

In this arrangement the R1C1 combination determines the free running frequency and the control voltage VC at pin 5 is set by voltage divider formed with R2 and R3. The initial voltage VC at pin 5 must be in the range

$$\frac{3}{4}(+V) \leq V_C \leq +V$$

Where +V is the total supply voltage.The modulating signal is ac coupled with the capacitor C and must be <3 VPP. The frequency of the output wave forms is approximated by

$$f_O \cong \frac{2(+V - V_C)}{R_1 C_1 (+V)}$$

where R1should be in the range 2KΩ < R1< 20KΩ. For affixed VC and constant C1, the **frequency fO can be varied over a 10:1 frequency range by the choice of R1 between 2KΩ < R1< 20KΩ.**

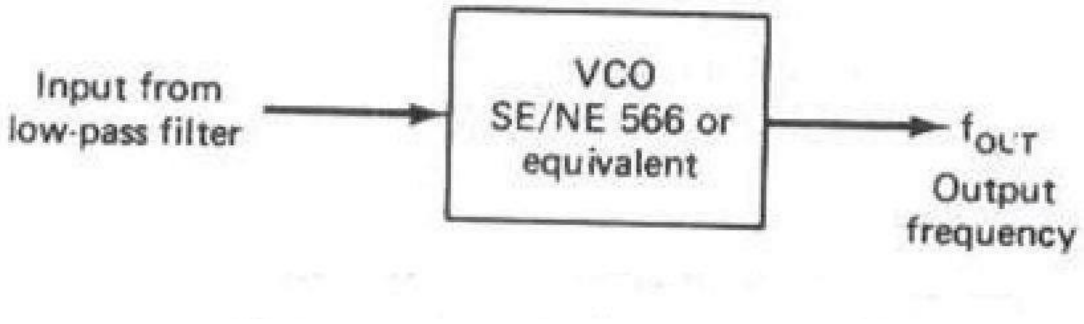


Fig 2.15: VCO Block Diagra

2.7 MONOLITHIC PHASE LOCK LOOPS IC 565:

Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM 560 series.

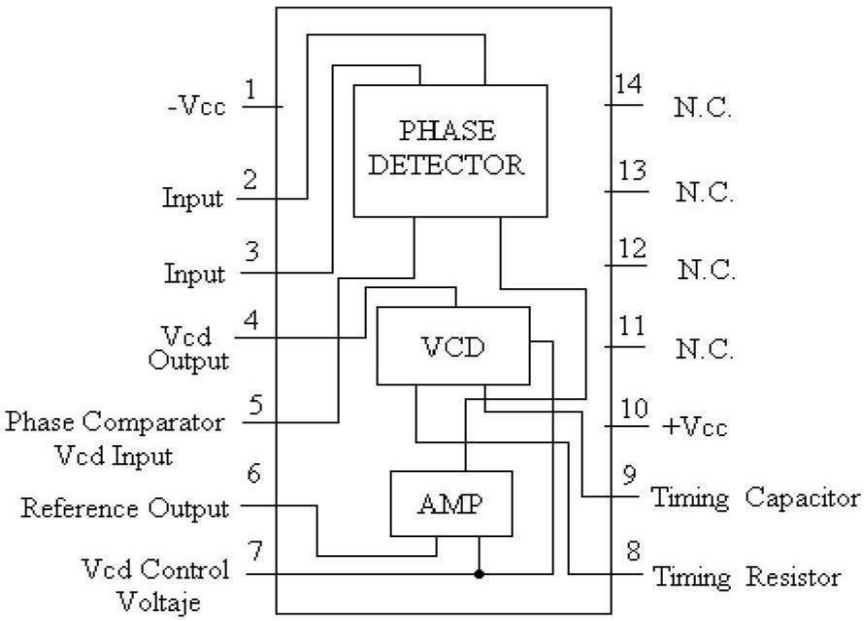


Fig 2.16: Pin configuration of IC 565

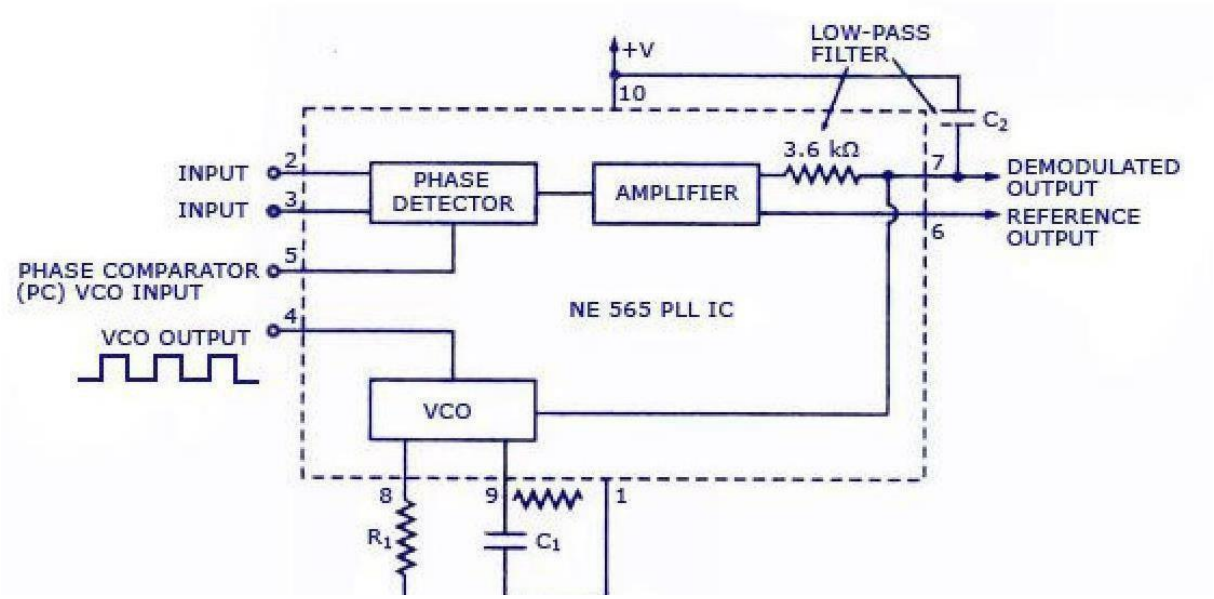


Fig 2.17: Block Diagram of IC 565

Fig 2.16 and 2.17 shows the pin diagram and block diagram of IC 565 PLL. It consists of phase detector, amplifier, low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore, it is necessary to connect output of VCO to the phase comparator input, externally. In frequency multiplication applications a digital frequency divider is inserted into the loop i.e., between pin 4 and pin 5. The centre frequency of the PLL is determined by the free-running frequency of the VCO and it is given by

$$f_o = \frac{1.2}{4R_1C_1}$$

Where R1 and C1 are an external resistor and capacitor connected to pins 8 and 9, respectively. The values of R1 and C1 are adjusted such that the free running frequency will be at the centre of the input frequency range. **The values of R1 are restricted from 2 kΩ to 20kΩ,but a capacitor can have any value.** A capacitor C2 connected between pin 7 and the **positive supply forms a first order low pass filter with an internal resistance of 3.6 kΩ.**

The value of filter capacitor C2 should be larger enough to eliminate possible demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t fo as the center frequency. The lock range fL and the capture range fC of the PLL are given by the following equations.

$$f_L = \pm\frac{8f_0}{V}$$

Where fo=free running frequency

V=(+V)-(-V)Volts

And

$$f_C = \pm\sqrt{\frac{f_L}{2\pi(3.6)10^3 C_2}}$$

From above equation the lock range increases with an increase in input voltage but decrease with increase in supply voltage. The two inputs to the phase detector allows direct coupling of an input signal, provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal.

UNIT-V

5.1 DATA CONVERTER INTEGRATED CIRCUITS

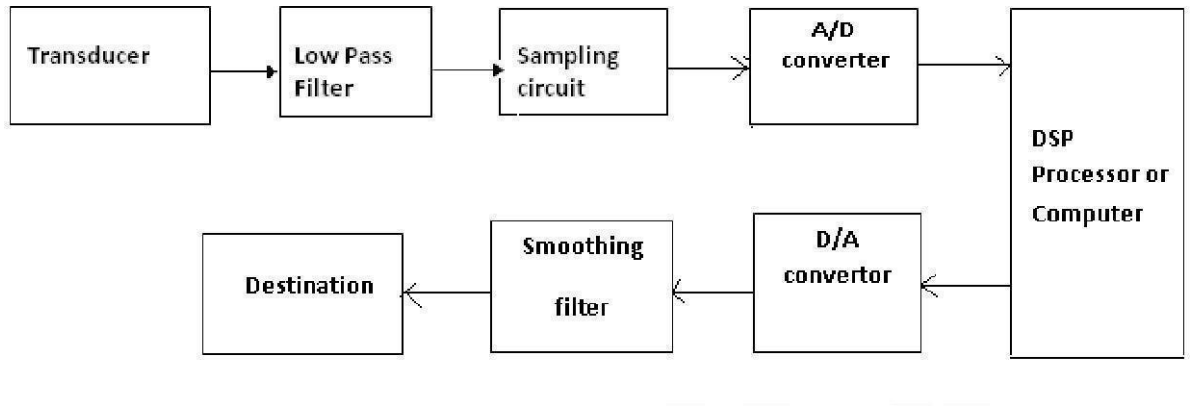


Fig: Application of A/D and D/A converters

Fig shows the application of A/D and D/A converters. The transducer circuit will gives an analog signal. This signal is transmitted through the LPF circuit to avoid higher components, and then the signal is sampled at twice the frequency of the signal to avoid the overlapping. The output of the sampling circuit is applied to A/D converter where the **samples are converted into binary data i.e. 0's and 1's. Like this the analog data converted** into digital data.

The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.

5.2. BASIC DAC TECHNIQUES

The input of the block diagram is binary data i.e, 0 and 1, it contain 'n' number of input bits designated as **d1,d2,d3,…..dn . this input is combined with the reference voltage** called Vref to give an analog output.

Where d1 is the MSB bit and dn is the LSB bit

Vo= Vref (d1*2-1+d2*2- 2+d3*2-**3+… .....+dn*2**-n)

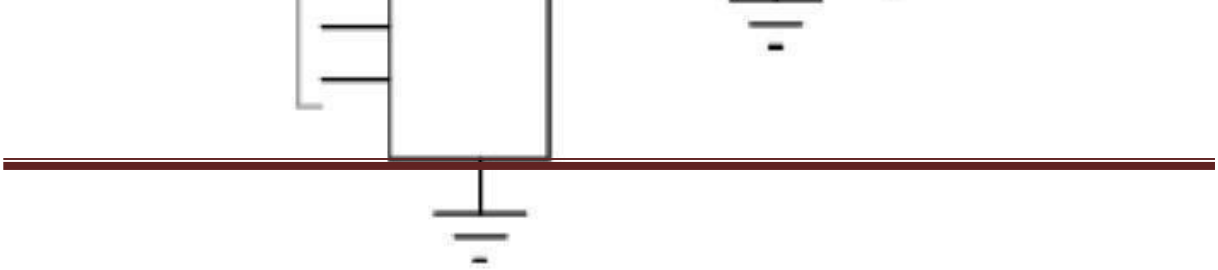


Fig: Basic DAC diagram

5.2.1 Weighted Resistor:

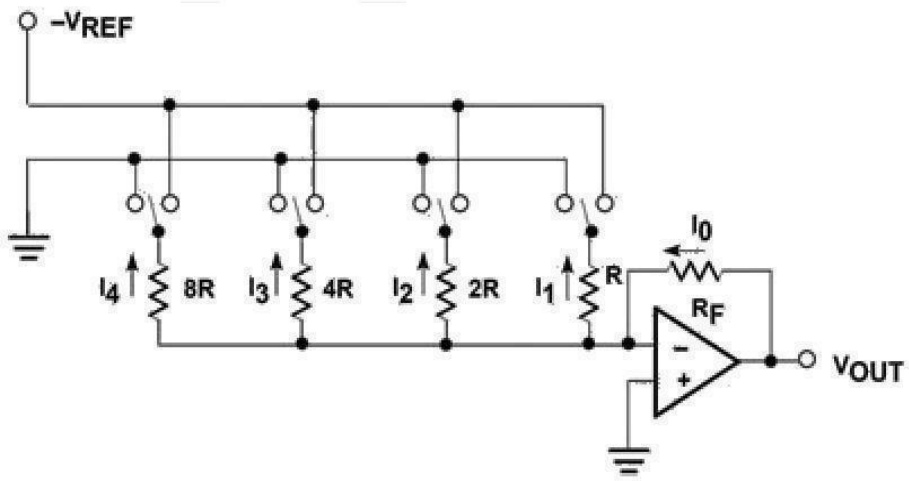


Fig: simple 4-bit weighted resistor

Fig. shows a simplest circuit of weighted resistor. It uses a summing inverting amplifier. It contains n- electronic switches (i.e. 4 switches) and these switches are controlled by binary input bits d1, d2, d3, d4. If the binary input bit is 1 then the switch is connected to reference voltage –VREF , if the binary input bit is 0 then the switch is connected to ground.

The output current equation is

Io=I1+I2+I3+I 4 Io= VREF (d1*2-1+d2*2-2+d3*2-3+d4*2-4)

The transfer characteristics are shown below (fig 2.13) for a 3-bit weighted resistor

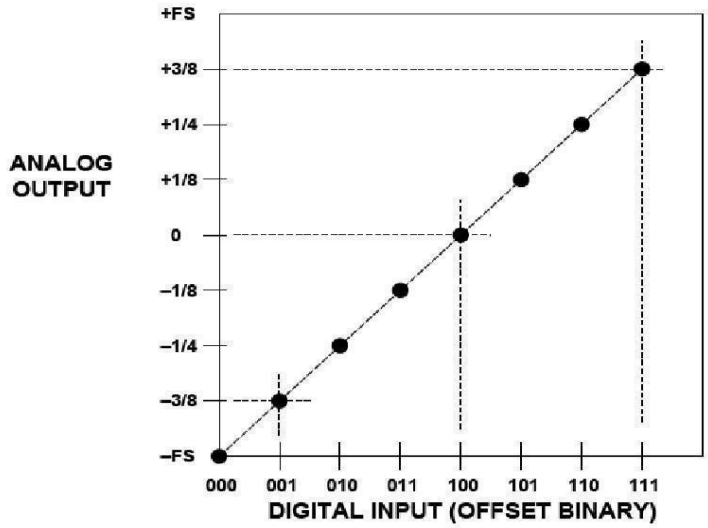


Fig: Transfer characteristics of 3-bit weighted resistor

Disadvantages of Weighted resistor D/A converter:

Wide range of resistor's are required in this circuit and it is very difficult to fabricate such a wide range of resistance values in monolithic IC. This difficulty can be eliminated using R-2R ladder network.

5.2.2 R-2R LADDER DAC

Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC. The circuit of R-2R ladder network is shown in fig. The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths. The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output. The inverting input of the op-amp is at virtual earth. Current flowing in the elements of the ladder network is therefore unaffected by switch positions.

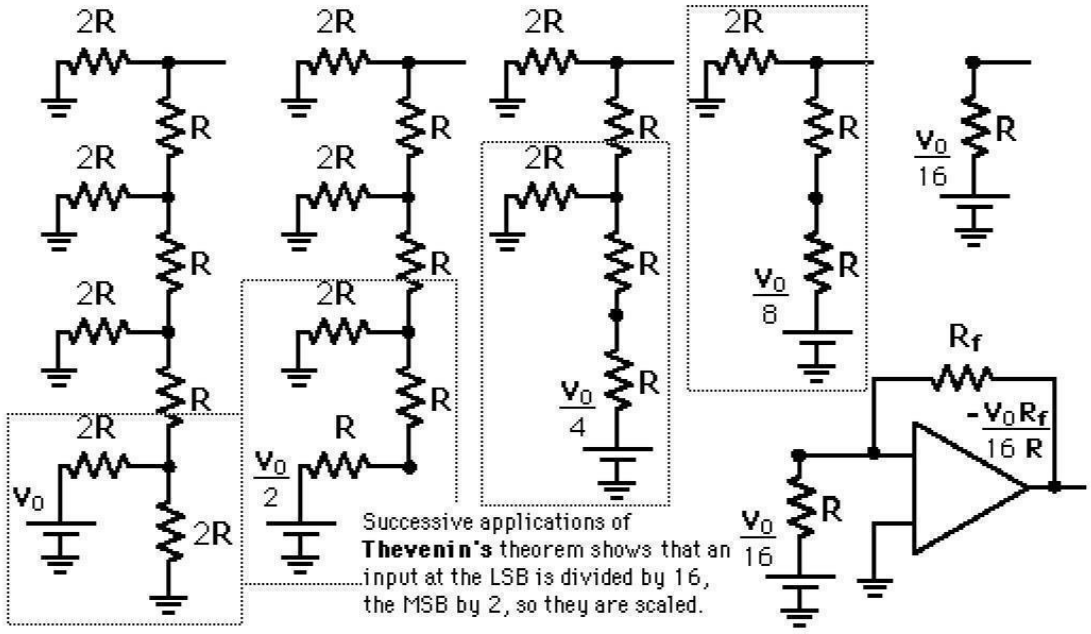


Fig: A 4-bit R-2R Ladder DAC

If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

$$Vout = Vr/2N$$

where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc.

Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

Vout = (Vr/2)+(Vr/8) which reduces to Vout = 5Vr/8.

An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt).

5.2.3 INVERTED R-2R LADDER DAC

In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC (fig 2.20)

In this MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of op-amp which is also at virtual ground. When the input binary in logic 1 then it is connected to the virtual ground, when input binary is logic 0 then it is connected to the ground i.e. the current flowing through the resistor is constant.

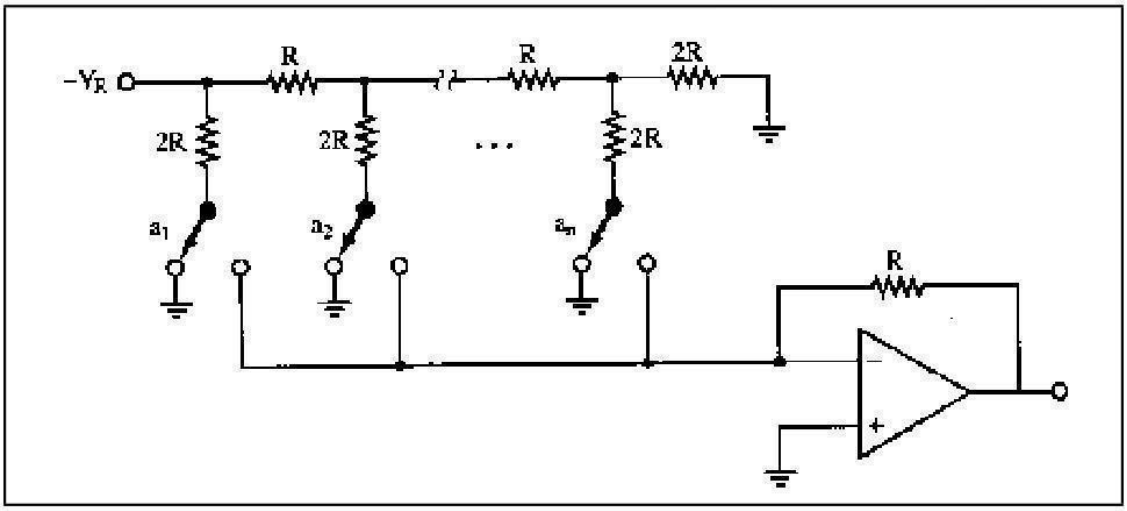


Fig Inverted R-2R ladder

5.3 DIFFERENT TYPES OF ADC'S

It provides the function just opposite to that of a DAC. It accepts an analog input voltage Va and produces an output binary word d1, d2,**d3….dn. Where d1 is the most significant bit and** dn is the least significant bit.

ADCs are broadly classified into two groups according to their conversion techniques

(1)Direct type

(2)Integrating type

Direct type ADCs compares a given analog signal with the internally generated equivalent signal. This group includes

i) Flash (Comparator) type converter

ii) Successive approximation type convertor

iii) Counter type

iv) Servo or Tracking type

Integrated type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code.

5.3.1. FLASH (COMPARATOR) TYPE CONVERTER:

A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N - 1, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output (by outputting an out-of-sequence code). Scaling to newer sub-micrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.

A Flash ADC (also known as a direct conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors; however modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital
encoder which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a unary value).

Also called the *parallel* A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

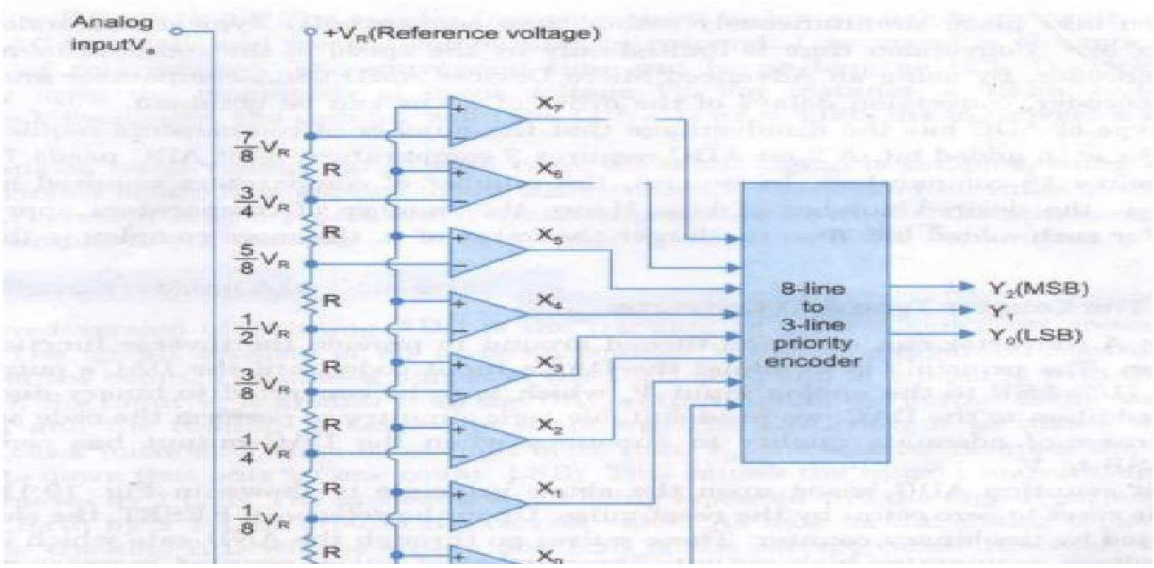
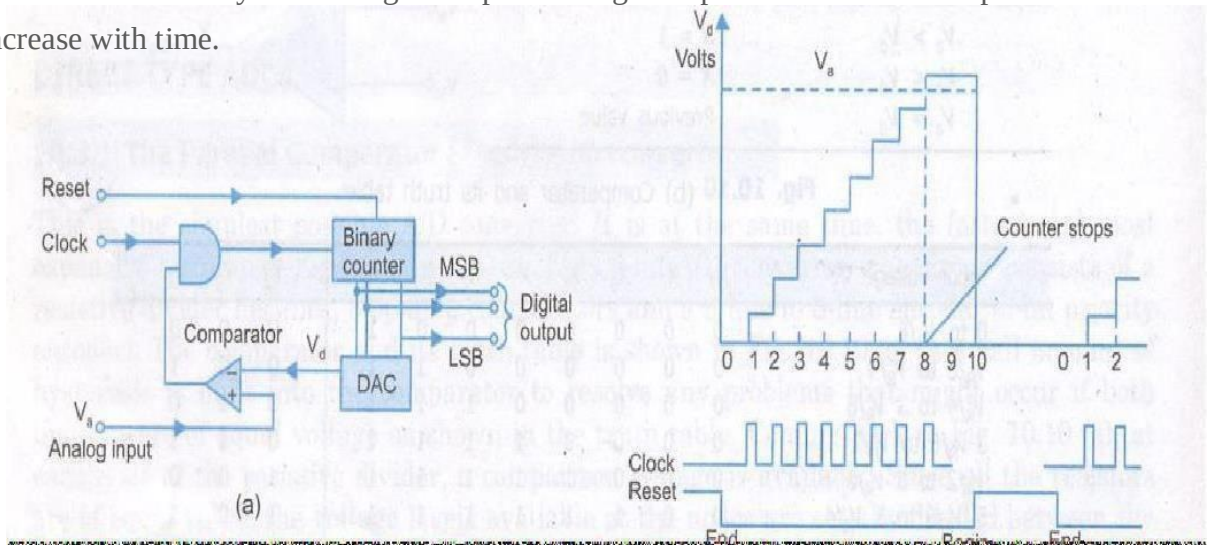


Fig 2.24: flash (parallel comparator) type ADC

VR is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic. As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

5.3.2 COUNTER TYPE A/D CONVERTER

In the fig 2.22 the counter is reset to zero count by reset pulse. After releasing the reset pulse the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time.



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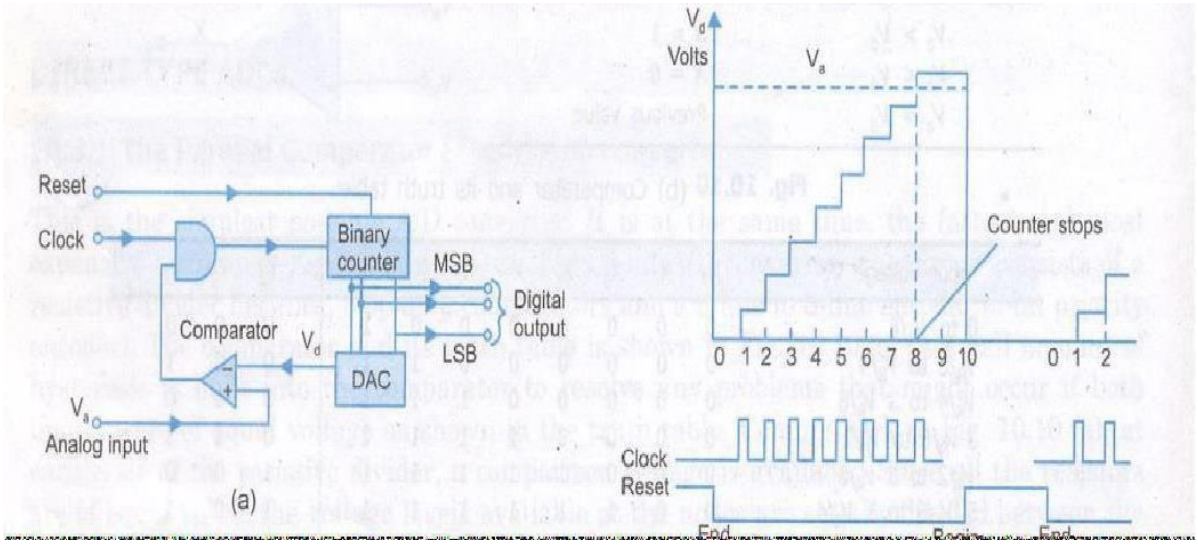

Fig 2.25: Countertype A/D converter

The binary word representing this count is used as the input of a D/A converter whose output is a stair case. The analog output Vd of DAC is compared to the analog input input Va by the comparator. If Va>Vd the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va<Vd the output of the comparator becomes low and the AND gate is disabled. This stops the counting we can get the digital data.

5.3.3 SERVO TRACKING A/D CONVERTER :

An improved version of counting ADC is the tracking or servo converter shown in fig 2.23. The circuit consists of an up/down counter with the comparator controlling the direction of the count.

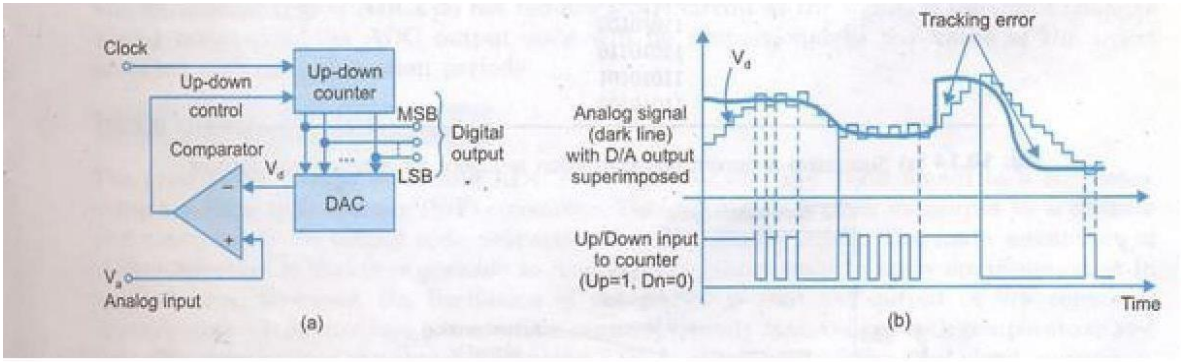

Fig: 2.26: (a) A tracking A/D converter (b) waveforms associated with a tracking A/D converter

The analog output of the DAC is Vd and is compared with the analog input Va. If the input Va is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse when it becomes more than Va the counter reverses the direction and counts down.

5.3.4 SUCCESSIVE-APPROXIMATION ADC:

One method of addressing the digital ramp ADC's shortcomings is the so-called successive-approximation ADC. The only change in this design as shown in the fig 2.19 is a very special counter circuit known as a successive-approximation register.

Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly. The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

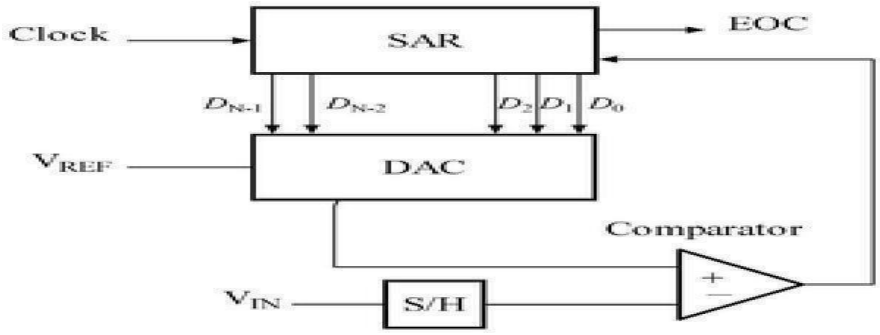

Fig: 2.27: Successive approximation ADC circuits

The successive approximation analog to digital converter circuit typically consists of four chief sub

1. A sample and hold circuit to acquire the input voltage (Vin).
2. An analog voltage comparator that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC.

4.An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

Mathematically, let Vin = xVref, so x in [-1, 1] is the normalized input voltage. The objective is to approximately digitize x to an accuracy of 1/2n. The algorithm proceeds as follows:

1. Initial approximation x0 = 0.

2.ith approximation xi = xi-1 - s(xi-1 - x)/2i.
where, s(x) is the signum-**function(sgn(x)) (+1 for x ≥ 0,** -1 for x < 0). It follows using mathematical induction that |xn - **x| ≤ 1/2n.**

As shown in the above algorithm, a SAR ADC requires:

1.An input voltage source Vin.

2.A reference voltage source Vref to normalize the input.

3.A DAC to convert the ith approximation xi to a voltage.

4.A Comparator to perform the function s(xi - x) by comparing the DAC's voltage with the input voltage.

5.A Register to store the output of the comparator and apply xi-1 - s(xi-1 - x)/2i.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons.

For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary search.

The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

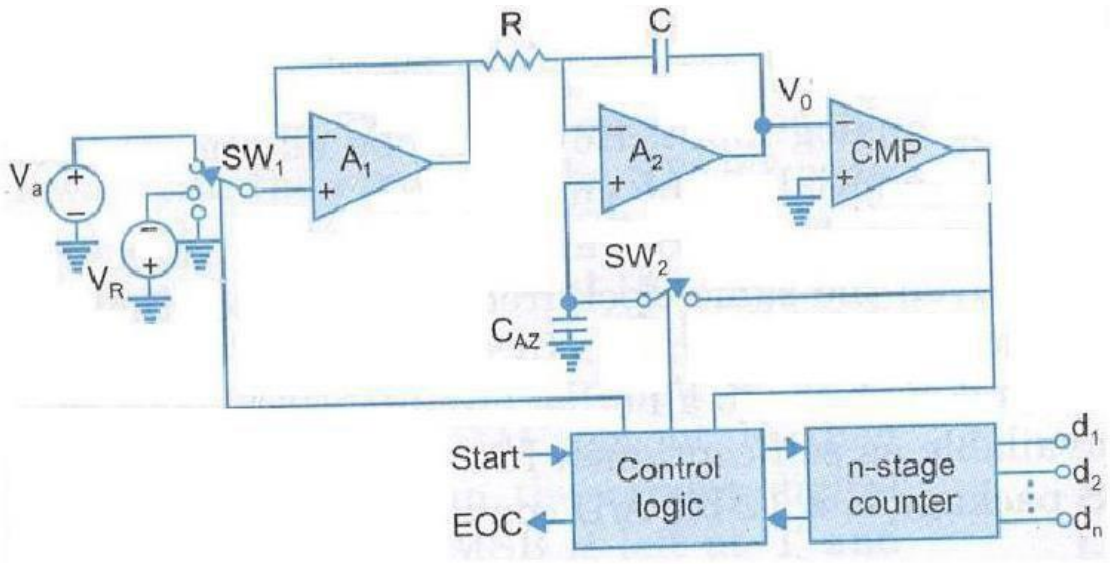

Fig 2.28: (a): Functional diagram of dual slope ADC

An integrating ADC (also **dual-slope** ADC) shown in fig 2.25

(a.) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

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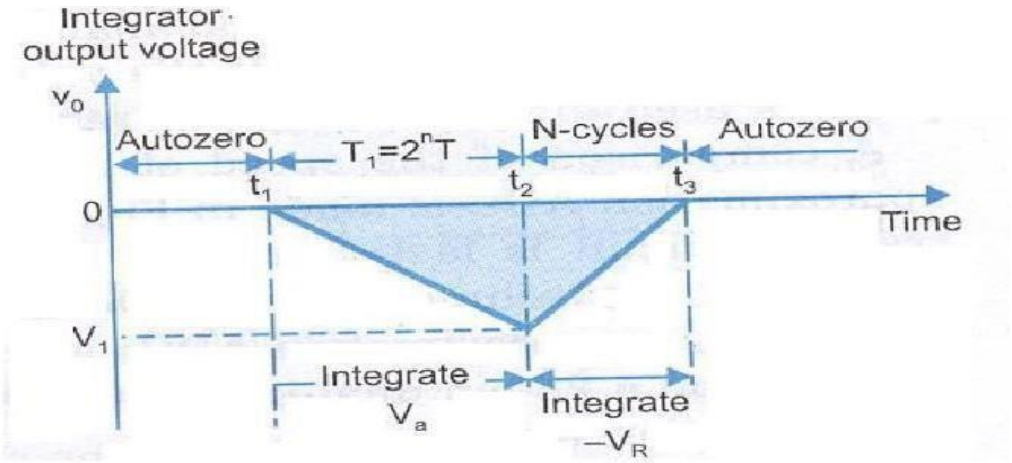

Fig 2.25 (b) o/p waveform of dual slope ADC

In operation the integrator is first zeroed (close SW2), then attached to the input (SW1 up) for a fixed time *M* counts of the clock (frequency 1/*t*). At the end of that time it is attached to the reference voltage (SW1 down) and the number of counts *N* which accumulate before the integrator reaches zero volts output and the comparator output changes are determined. The waveform of dual slope ADC is shown in fig 2.25 (b). The equations of operation are therefore:

$$T_1 = t_2 - t_1 = \frac{2^n\ counts}{clock\ rate}$$

And

$$t_3 - t_2 = \frac{digitalcountN}{clockrate}$$

For an integrator,

$$\Delta V_O = \frac{-1}{RC} V(\Delta t)$$

The voltage Vo will be equal to V1 at the instant t2 and can be written as

$$V_1 = \frac{-1}{RC} V_a (t_2 - t_1)$$

The voltage V1 is also given by

$$V_1 = \frac{-1}{RC}(-V_R)(t_2 - t_3)$$

So,

$$V_a(t_2 - t_1) = (V_R)(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and, we get

$$V_a(2^n) = (V_R)N$$

Or,

$$V_a = (V_R)\left(\frac{N}{2^n}\right)$$

5.4. SPECIFICATIONS FOR DAC/ADC

1. RESOLUTION: The Resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

Resolution (in volts)=(VFS)/(2n-1)= 1 LSB increment

Ex: An 8-bit D/A converter have 28-1=255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range.

An 8-bit DAC is said to have: 8 bit resolution

:a resolution of 0.392 of full scale

:a resolution of 1 part in 255

Similarly the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

Ex: the input range of 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.22 mV = (10V/255)

2. LINEARITY: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal characteristics.

3. GLITCHES (PARTICULARLY DAC): In transition from one digital input to the next, like

0111 to 1000, it may effectively go through 1111 or 0000, which produces ―unexpected‖

voltage briefly. If can cause problems elsewhere.

4. ACCURACY: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

5. MONOTONIC: A monotonic DAC is the one whose analog output increases for an increase in digital input. It is essential in control applications. If a DAC has to be monotonic, the error should de lessthan ±(1/2) LSB at each output level.

6. SETTLING TIME: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances.
Its ranges from 100ns to **10µs.**

7. STABILITY: The performance of converter changes with temperature, age and power supply variations. So the stability is required.

ALL THE BEST